Specification For HINK 42''EPD

Model NO.: HINK-E420A01

Product VER:A1

Customer Approval

Customer	
Approval By	
Date Of Approval	

It will be agreed by the receiver,if not sign back the Specification within 15days.

Prepared By	Checked By	Approval By
Daisy Zhu	Yufeng Zhou	Ziping Hu

Version	Content	Date	Producer
A0	New release	2018/09/07	Wang Lin
A1	Update the PCBA size	2022/03/16	Daisy Zhu

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1.General Description

HINK-E420A01 i is a reflective electrophoretic technology display module based on active matrix TFT substrate. It has 42” active area with 2160 x 2880 pixels and 3:4 aspect ratios. The display is capable to display images at 2-16 gray levels (1-4 bits) depending on the display controller and the associated waveform file it used.

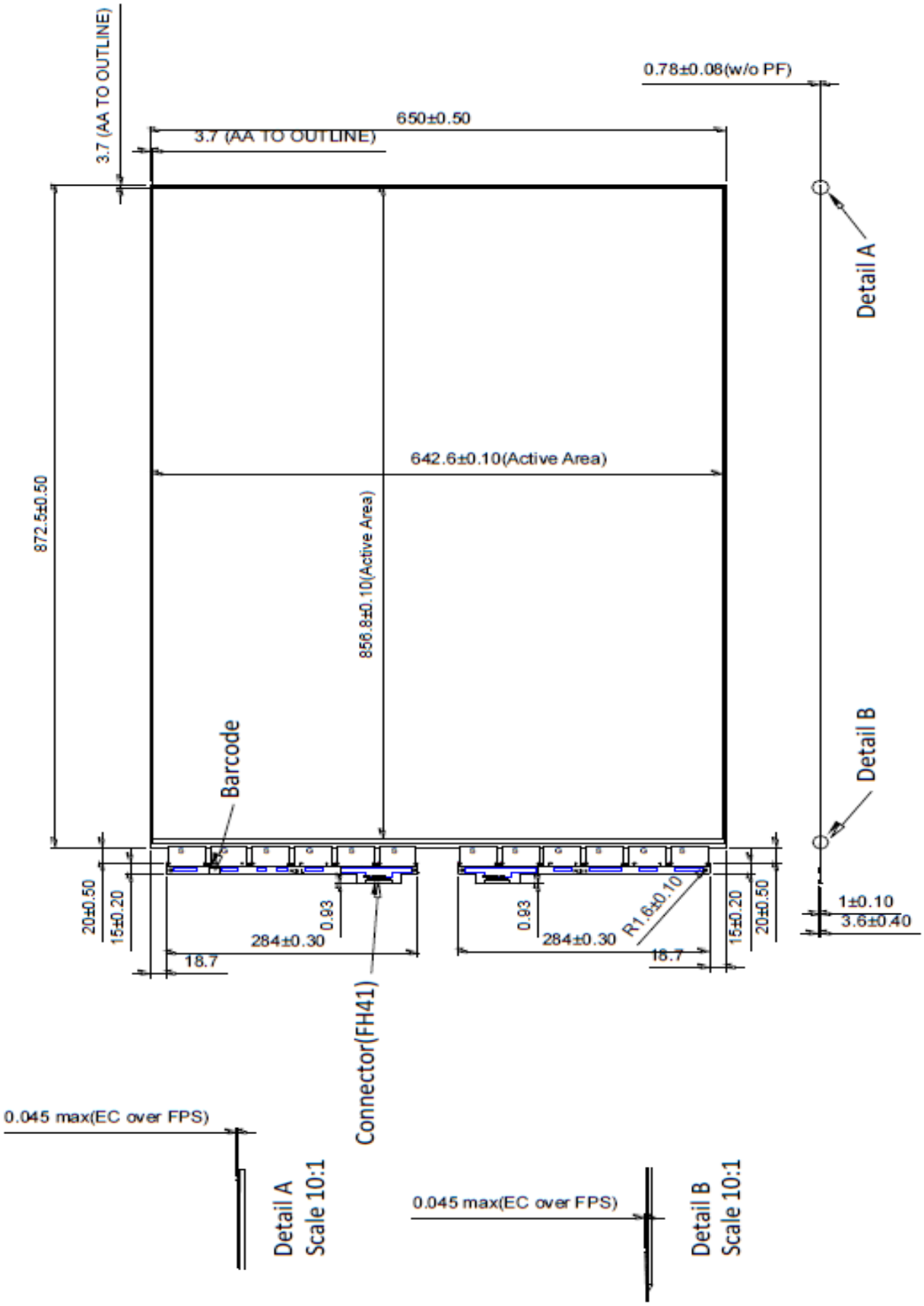
2.Features

- 2160×2880 resolution
- High contrast
- High reflectance
- Ultra wide viewing angle
- Ultra low power consumption
- Pure reflective mode
- Image stable
- Landscape/Portrait mode
- Bi-stable display
- Commercial temperature range：0-50℃
- Landscape mode

3.Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	42	Inch	
Display Resolution	2160(H) x 2880(V)	Pixel	3:4
Active Area	642.6(H) x 856.8 (V)	mm	
Pixel Pitch	0.2975	mm	
Pixel Configuration	Square		
Outline Dimension	650(H) x 872.5 (V) x 0.805(D)	mm	w/o masking film
Module Weight	1100 ±20	g	
Display operating mode	Reflective mode		
Surface treatment	Hard coat		

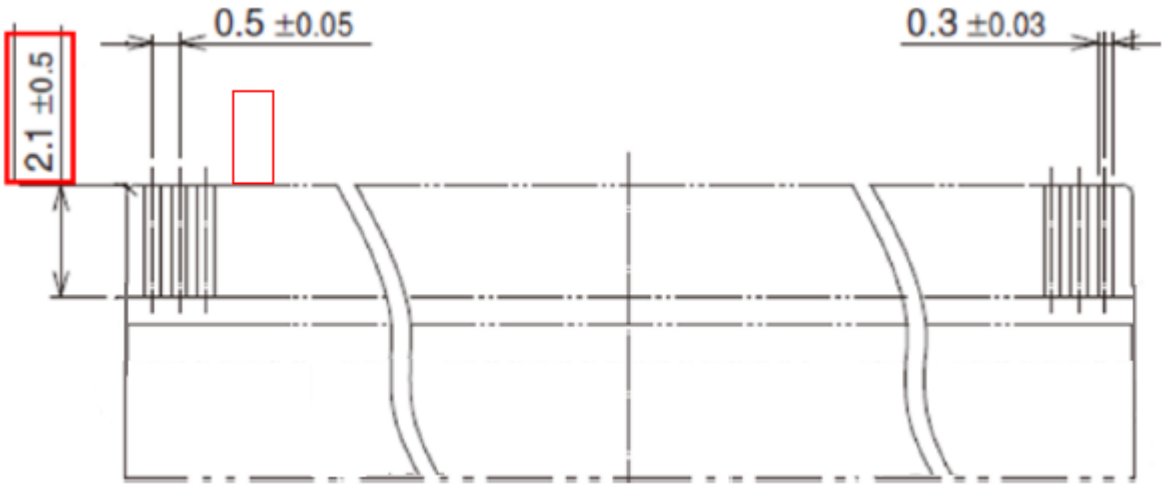
4.Mechanical Drawing of EPD module



5.Input/Output Terminals

5.1 Connector type: FH41-50S-0.5SH compatible.

Note 5-1: Recommended the lead length of the FFC is2.1mm. (The FFC drawing below is only for reference.)



5.2 Pin Assignment

1) PCB-L

Pin #	Signal	Description
1	VGL	Negative power supply gate driver
2	NC	Please keep the pin floating
3	VGH	Positive power supply gate driver
4	Mode2_L	Output enable gate driver
5	VDD	Digital power supply drivers
6	Mode1_L	Output enable gate driver
7	CKV_L	Clock gate driver
8	SPV_L	Start pulse gate driver
9	VSS	Ground
10	VCOM TFT	Common voltage
11	VDD	Digital power supply drivers
12	VSS	Ground
13	XCL_L	Clock source driver
14	D0	Data signal source driver
15	D1	Data signal source driver
16	D2	Data signal source driver
17	D3	Data signal source driver
18	D4	Data signal source driver
19	D5	Data signal source driver
20	D6	Data signal source driver
21	D7	Data signal source driver
22	VSS	Ground
23	D8	Data signal source driver

24	D9	Data signal source driver
25	D10	Data signal source driver
26	D11	Data signal source driver
27	D12	Data signal source driver
28	D13	Data signal source driver
29	D14	Data signal source driver
30	D15	Data signal source driver
31	NC	Please keep the pin floating
32	XLE_L	Latch enable source driver
33	XOE_L	Outputs enabled when OE is logic “H”,
34	ISEL	Input data bus width selection.
35	NC	Please keep the pin floating
36	VPOS	Positive power supply source driver
37	NC	Please keep the pin floating
38	VNEG	Negative power supply source driver
39	VCOM FPL	Common voltage
40	NC	Please keep the pin floating
41	NC	Please keep the pin floating
42	NC	Please keep the pin floating
43	NC	Please keep the pin floating
44	NC	Please keep the pin floating
45	NC	Please keep the pin floating
46	NC	Please keep the pin floating
47	NC	Please keep the pin floating
48	NC	Please keep the pin floating
49	NC	Please keep the pin floating
50	XSTL_L	Start pulse source driver

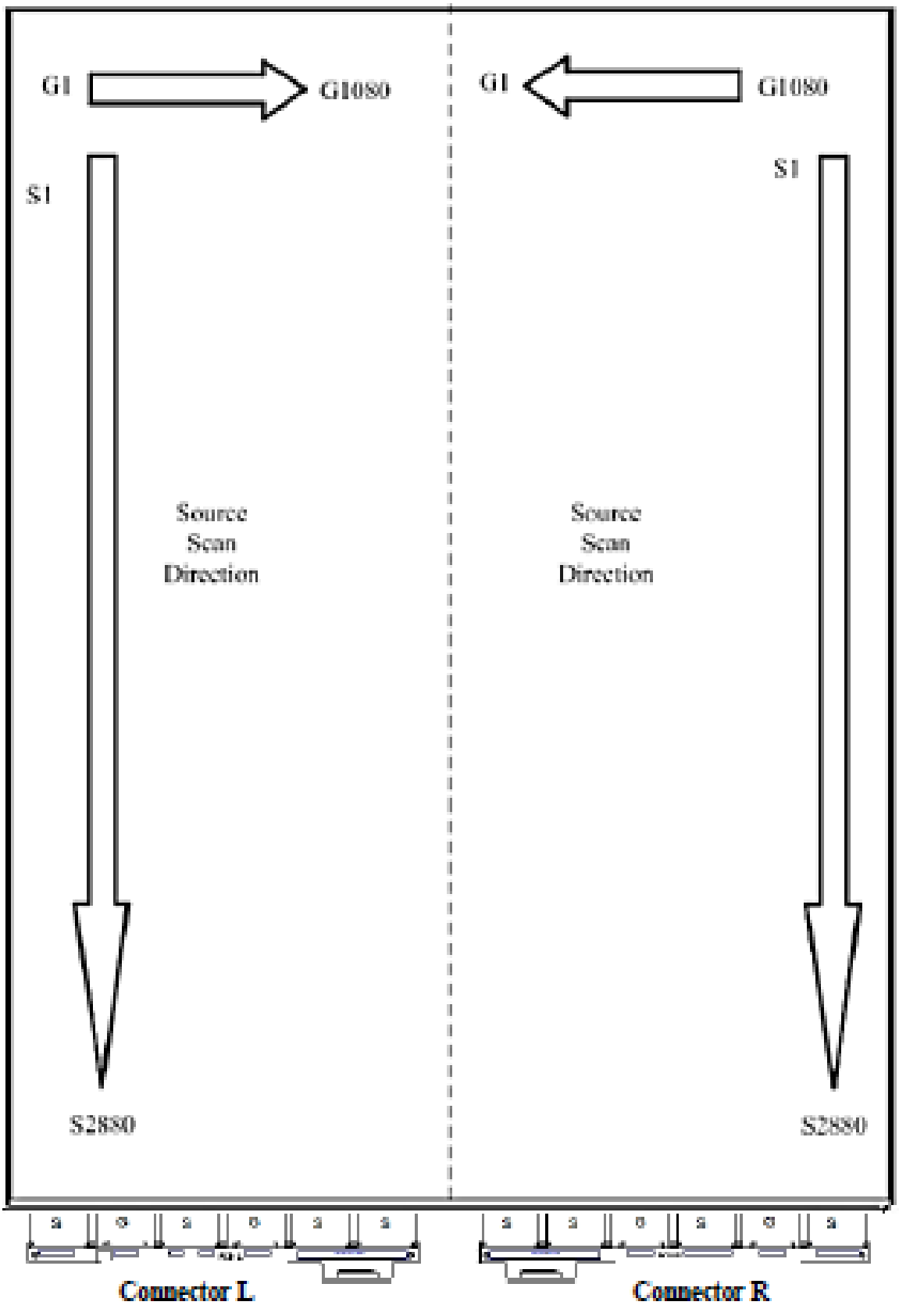
2) PCB-R

Pin #	Signal	Description
1	VGL	Negative power supply gate driver
2	NC	Please keep the pin floating
3	VGH	Positive power supply gate driver
4	Mode2_R	Output mode selection gate driver
5	VDD	Digital power supply drivers
6	Mode1_R	Output mode selection gate driver
7	CKV_R	Clock gate driver
8	NC	Please keep the pin floating
9	VSS	Ground
10	VCOM TFT	Common voltage
11	VDD	Digital power supply drivers
12	VSS	Ground
13	XCL_R	Clock source driver

14	D0	Data signal source driver
15	D1	Data signal source driver
16	D2	Data signal source driver
17	D3	Data signal source driver
18	D4	Data signal source driver
19	D5	Data signal source driver
20	D6	Data signal source driver
21	D7	Data signal source driver
22	VSS	Ground
23	D8	Data signal source driver
24	D9	Data signal source driver
25	D10	Data signal source driver
26	D11	Data signal source driver
27	D12	Data signal source driver
28	D13	Data signal source driver
29	D14	Data signal source driver
30	D15	Data signal source driver
31	XSTL_R	Start pulse source driver
32	XLE_R	Latch enable source driver
33	XOE_R	Outputs enabled when OE is logic “H”
34	ISEL	Input data bus width selection.
35	NC	Please keep the pin floating
36	VPOS	Positive power supply source driver
37	NC	Please keep the pin floating
38	VNEG	Negative power supply source driver
39	VCOM FPL	Common voltage
40	NC	Please keep the pin floating
41	SPV_R	Start pulse gate driver
42	NC	Please keep the pin floating
43	NC	Please keep the pin floating
44	NC	Please keep the pin floating
45	NC	Please keep the pin floating
46	NC	Please keep the pin floating
47	NC	Please keep the pin floating
48	NC	Please keep the pin floating
49	NC	Please keep the pin floating
50	NC	Please keep the pin floating

5.2 Panel Scan Directions

When panel replace the image, each sub panel need to be active at the same time.



6. Display Module Electrical Characteristics

6.1 Absolute maximum rating

Table 6-1 Absolution maxing rating: The conditions in the table should not be exceeded; otherwise, the panel may be damaged.

Parameter	Symbol	Rating	Unit
Logic Supply Voltage	VDD	-0.3 to +7	V
Positive Supply Voltage	V_{POS}	-0.3 to +18	V
Negative Supply Voltage	V_{NEG}	+0.3to -18	V
Max .Drive Voltage Range	V_{POS} - V_{NEG}	36	V
Supply Voltage	VGH	-0.3 to +55	V
Supply Voltage	VGL	-32 to +0.3	V
Supply Range	VGH-VGL	-0.3 to +55	V
Operating Temp. Range	TOTR	0 to +50	℃
Storage Temperature	TSTG	-25 to +70	℃

6.2 Panel DC characteristics

Table 6-2 Panel DC characteristics: Please follow the table for the normal operation of the panel; otherwise, it may influence the panel's optical performance.

The standby power (PSTBY) is the consumed power when the panel controller is in standby mode. This value is only for reference since it depends on the performance of the panel controller.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Signal ground	VSS			0		V
Logic voltage supply	VDD		2.7	3.3	3.6	V
	IvDD	VDD=3.3V		78	84	mA
Gate negative supply	VGL		-21	-20	-19	V
	IGL	VGL= -20V		6	6	mA
Gate Positive supply	VGH		26	27	28	V
	IGH	VGH=27V		6	6	mA
Source negative supply	VNEG		-15.4	-15	-14.6	V
	INEG	VNEG= -15V	-	16	778	mA
Source positve supply	VPOS		14.6	15	15.4	V
	IPOS	VPOS=15v		18	780	mA
Asymmetry source	VAsym	VPOS+VNEG	-800	-	800	mV
Common voltage	Vcom		-2	Adjusted	-1	V
	Icom		-	2	-	mA
Panel Power	P		-	1024	23894	mW
Standby power panel	PSTBY		-	-	112	mW
Rush Currents	IDD	VDD=3.3V	-620		620	mA
	IGL	VGL=-20V	-1640		1640	mA
	IGH	VGH=27V	-480		480	mA
	INEG	VNEG=-15V	-1000			mA
	IPOS	VPOS=15V			1000	mA
	ICOM		-870		870	

- The maximum power consumption is measured using 50Hz waveform with following pattern transition: from pattern of repeated 1 consecutive black scan lines followed by 1 consecutive white scan line to that of repeated 1 consecutive white scan lines followed by 1 consecutive black scan lines. (Note 6-1)

- The Typical power consumption is measured using 50Hz waveform with following pattern transition: from horizontal 4 gray scale pattern to vertical 4 gray scale pattern. (Note 6-2)

- The standby power is the consumed power when the panel controller is in standby mode which here VDD is ON while other power supplies are OFF.

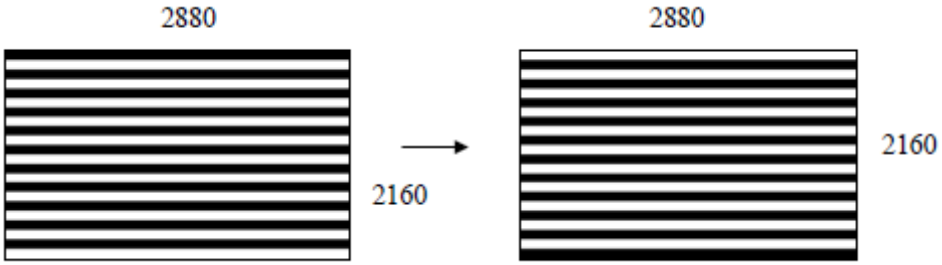
- The listed electrical/optical characteristics are only guaranteed under the panel controller & waveform provided by E Ink.

- Vcom is recommended to be set in the range of assigned value ±0.1V.

- The rush current is for reference only since it depends on the driving capacity of the panel controller.

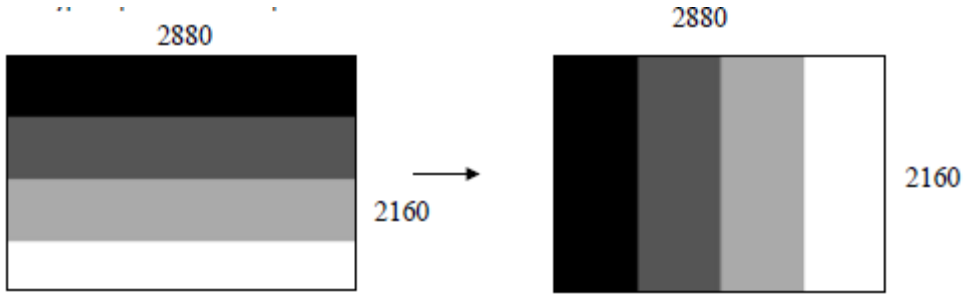
Note 6-1

The Maximum power consumption



Note 6-2

The Typical power consumption



6.3 Refresh Rate

The module Polaris is applied at a maximum screen refresh rate of 50Hz.

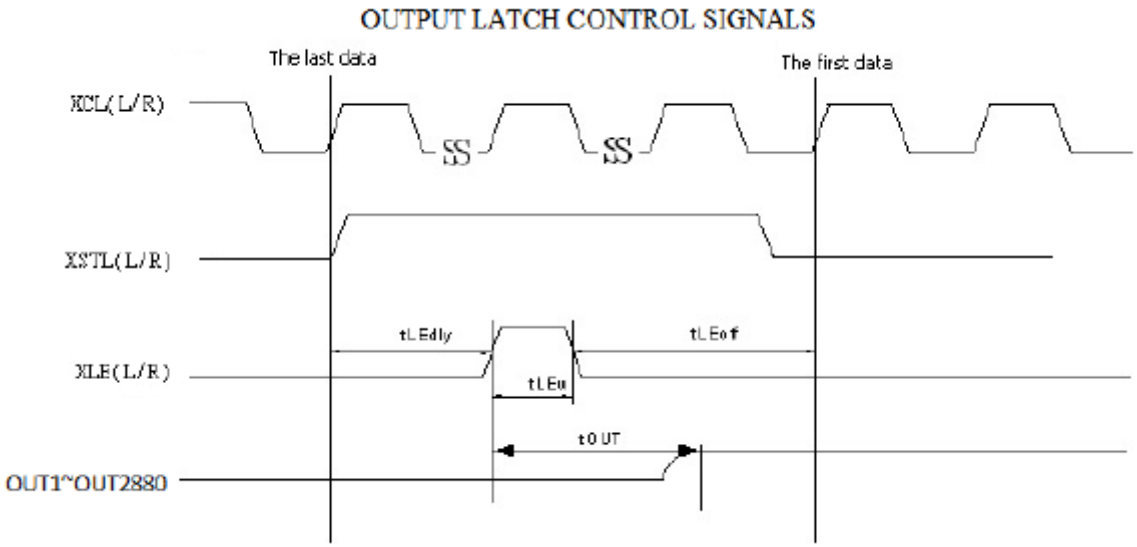
	Min	Max
Refresh Rate	-	50 Hz

6.4 Panel AC characteristics

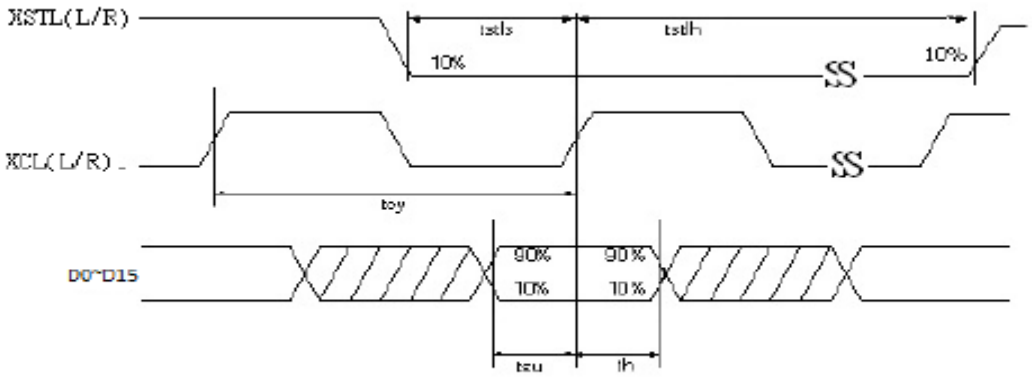
VDD=2.7V to 3.6V, unless otherwise specified.

The timing parameter for each sub panel

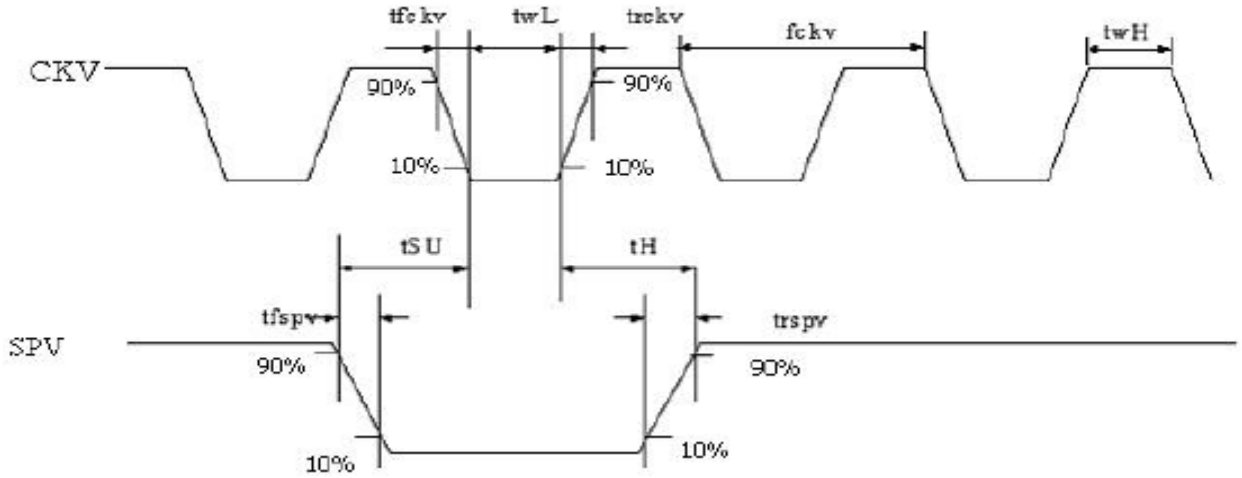
Parameter	Symbol	Min.	Typ.	Max.	Unit
Clock frequency	fckv			200	kHz
Minimum "L" clock pulse width	twL	0.5			us
Minimum "H" clock pulse width	twH	0.5			us
Clock rise time	trckv			100	ns
Clock fall time	tfckv			100	ns
SPV setup time	tSU	100	-	twH-100	ns
SPV hold time	tH	100	-	twH-100	ns
Pulse rise time	trspv	-	-	100	ns
Pulse fall time	tfspv	-	-	100	ns
Clock XCL cycle time	tcy	16.7	20		ns
D0 .. D15 setup time	tsu	8			ns
D0 .. D15 hold time	th	8			ns
XSTL setup time	tstls	8			ns
XSTL hold time	tstlh	8			ns
XLE on delay time	tLEdly	40			ns
XLE high-level pulse width (When VDD=2.7V to 3.6V)	tLEw	40			ns
XLE off delay time	tLEoff	200			ns



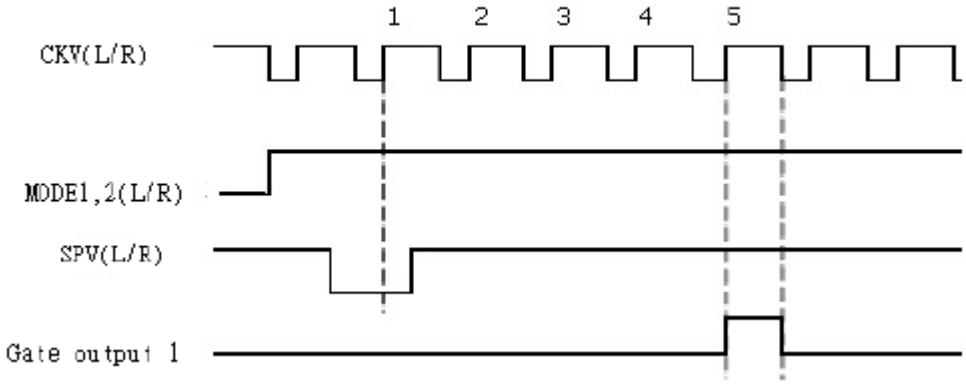
CLOCK & DATA TIMING



CKV & SPV TIMING



GATE OUTPUT TIMING



Note 6-3: First gate line on timing
After 5CKV, Gate output 1 is on.

6.5 Controllers Timing

This timing mode is depicted on Figure 1 and Figure 2 and it refers to timing of Source Driver Output Enable (SDOE)(3) and Gate Driver Clock (GDCK)(3). Note, that in this mode LGON follows GDCK timing.

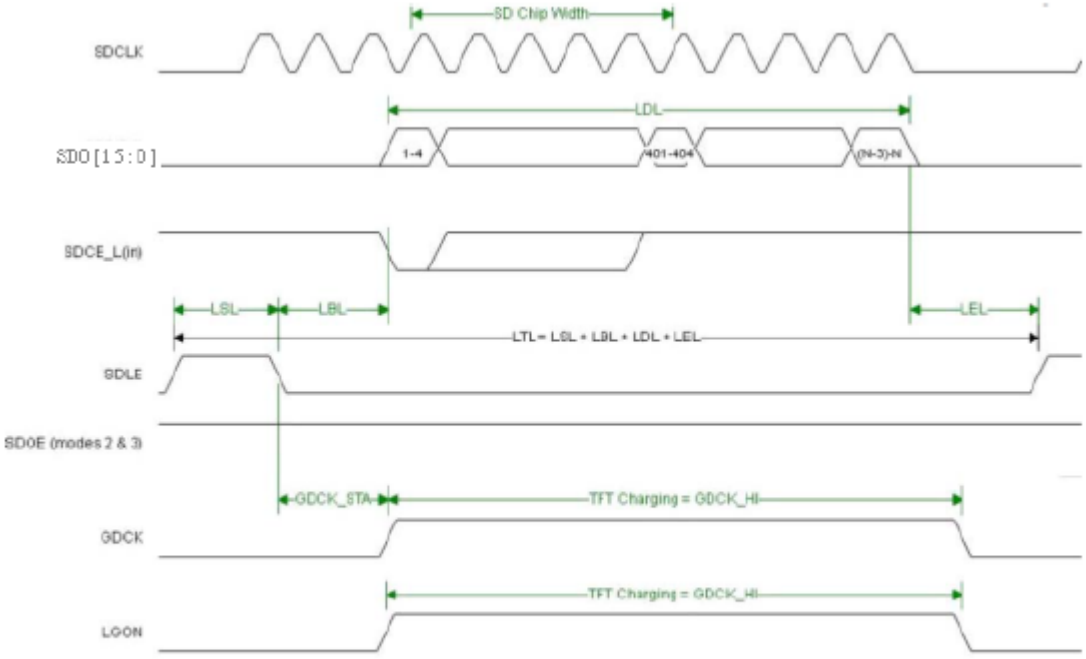


Figure 1 Line Timing in Mode 3

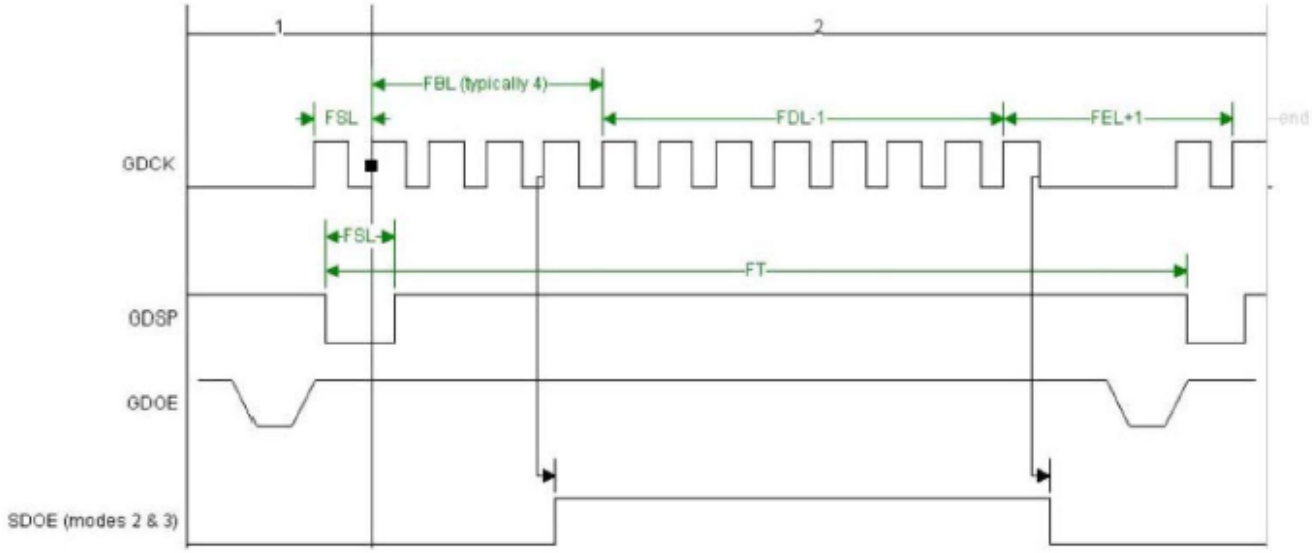


Figure 2 Frame Timing in Mode 3

6.6Table Timing Parameters Table

Table Timing Parameters Table (For 1 panel)

Mode	3	Timing				
SDCLK[MHz]	42.00	Resolution			5760x1080	
Pixels per SDCLK	8					
Line Parameters [SDCLK]	LSL	LBL	LDL	LEL	GDCK_STA	LGONL
	1	5	720	40	37	630
Line Parameters [us]	0.02	0.12	17.14	0.95	0.88	15.04
Frame Parameters [Lines]	FSL	FBL	FDL	FEL	-	FR[Hz]
	1	4	1080	15	-	49.84
Frame Parameters[us]	18.23	72.95	19697	273.57	-	-

Note 1: For parameters definition, see Section 7. Active Matrix Electronic Paper Display Timings.
Note 2: For Freescale SoC GDOE Low pulse represent FSL and GDSP pulses with the first period of FBL
Note 3:

SDCLK = XCL(L /R)
SDD [15:0] = D0~D15(L/R)
SDCE_L(in) = XSTL(L /R)
GDCK = CKV(L /R)
GDSP = SPV(L /R)
GDOE = Mode1、2(L /R)
SDOE = XOE(L/R)

7. Power Sequence

Power Rails must be sequenced in the following order:

1. VSS → VDD →VNEG →VPOS(Source driver) → VCOM
2. VSS →VDD → VGL → VGH (Gate driver)

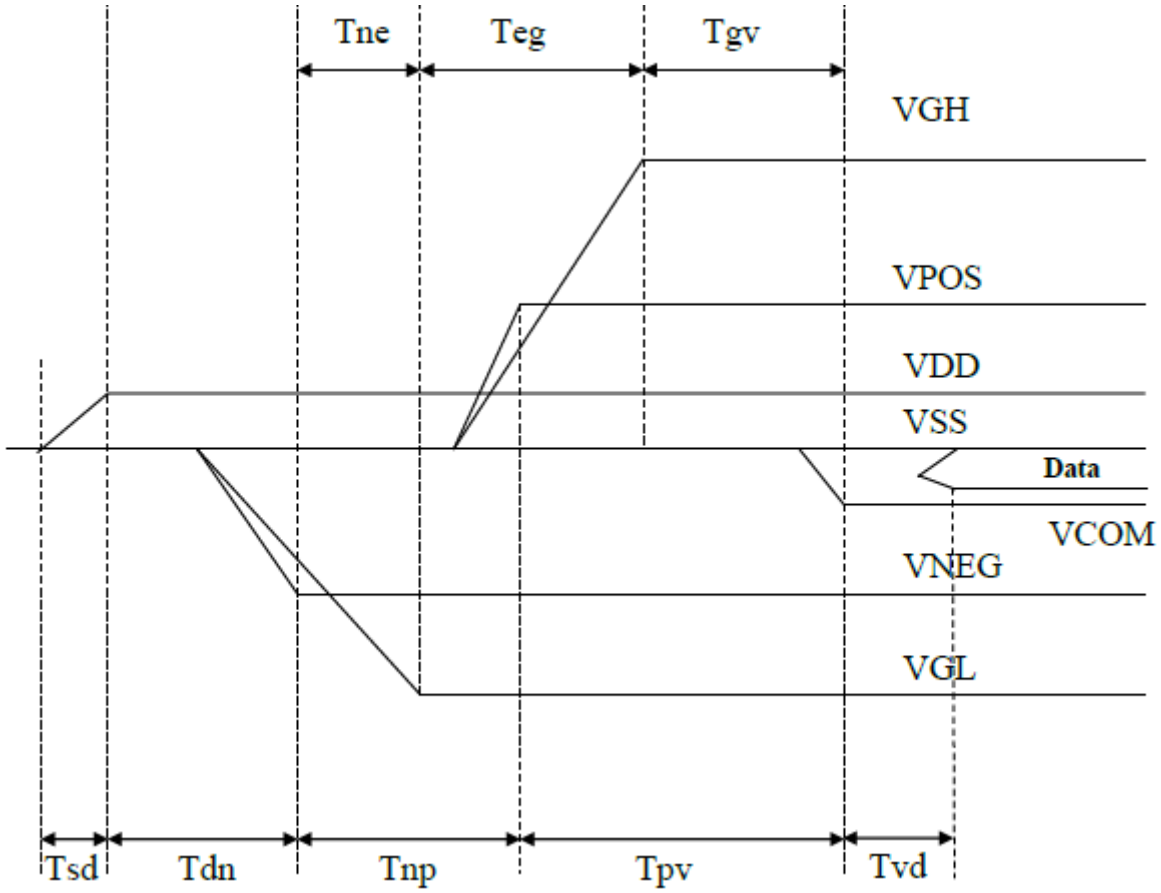
Note7-1:

•VGL should be turned off after VNEG and VPOS have been turned off and returned to the ground state.

•VGL should be turned off after the Vcom has been turned off and returned to the ground state.

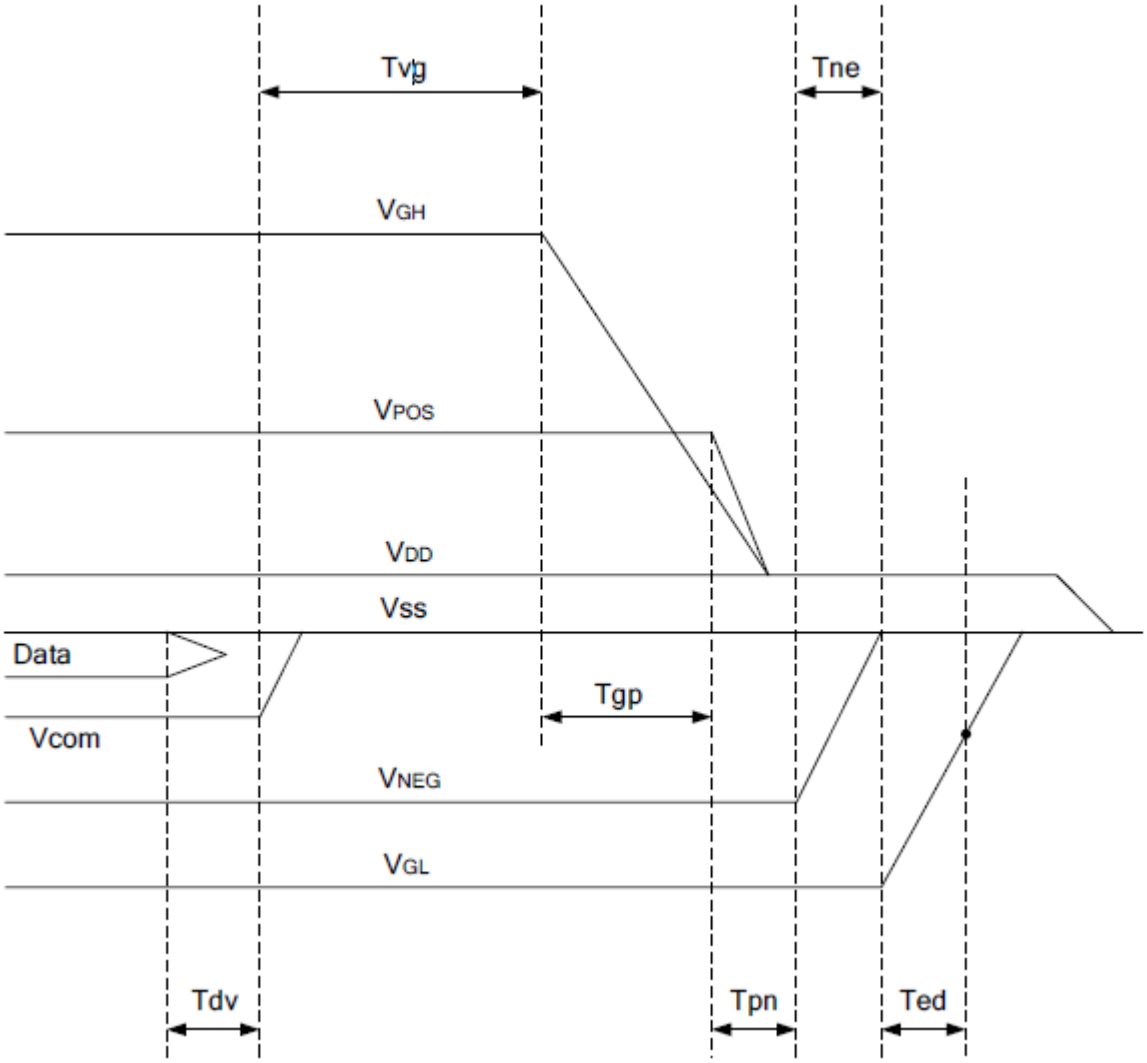
•All of Vcom/VNEG/VPOS/VGN/VGL MUST turn off right after data transfer completes.

POWER ON



	Min	Max
Tsd	30us	-
Tde	100us	-
Tep	1000us	-
Tpv	100us	-
Tvd	100us	-
Ten	0us	-
Tng	1000us	-
Tgv	100us	-

POWER OFF



	Min	Max	Remark
Tdv	100μs	-	-
Tvg	0μs	-	-
Tgp	0μs	-	-
Tpn	0μs	-	-
Tne	0μs	-	-
Ted	0.5s	-	Discharged point @ -7.4 Volt

•Note7-2: Supply voltages decay through pull-down resistors.

8. Optical characteristics

8.1 Specification

Measurements are made with that the illumination is under an angle of 45 degrees, the detector is perpendicular unless otherwise specified.

T=25±2℃

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT	Note
R	Reflectance	White	30	40	--	%	Note8-1
Gn	Nth Grey level	-	-	DS+(WS-DS)×n(m-1）	-	L*	--
CR	Contrast Ratio	-	10	12	-		--

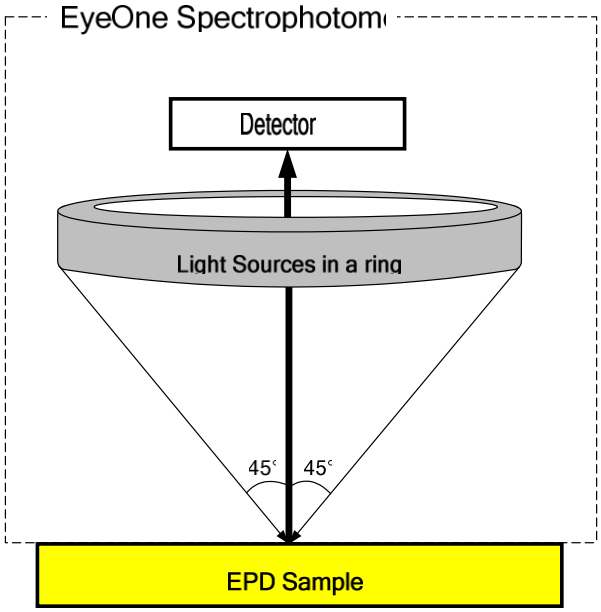
WS: White state , DS: Dark state, Gray state from Dark to White :DS、G1、G2…、Gn…、Gm-2、WSm:4、8、16 when 2、3、4 bits mode

Note 8-1：Luminance meter：Eye － One Pro Spectrophotometer

8. 2 Definition of contrast ratio

The contrast ratio (CR) is the ratio between the reflectance in a full white area (Rl) and the reflectance in a dark area (Rd):

CR = Rl/Rd

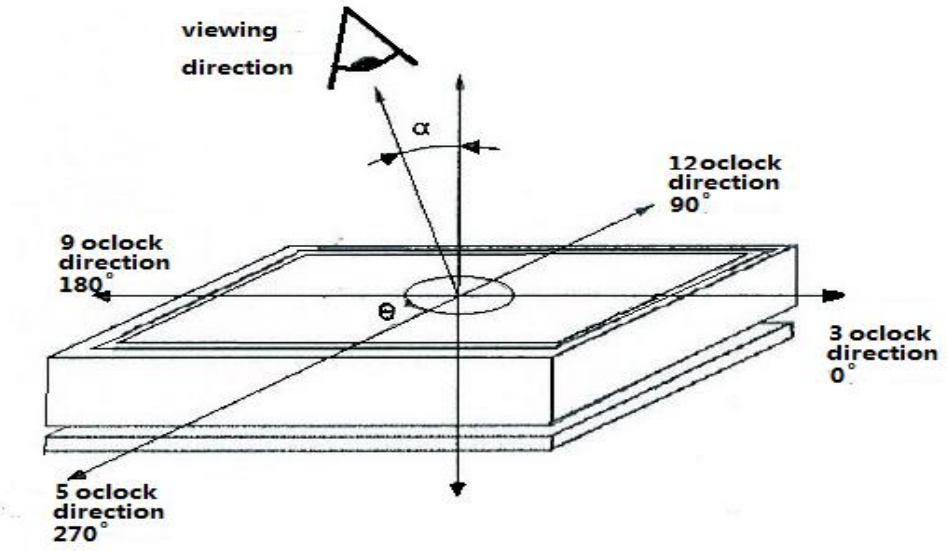


8. 3 Reflection Ratio

The reflection ratio is expressed as:

R = Reflectance Factor $_{\text{white board}}$ x (L_{center} / $L_{\text{white board}}$)

L_{center} is the luminance measured at center in a white area (R=G =B=1). $L_{\text{white board}}$ is the luminance of a standard white board. Both are measured with equivalent illumination source. The viewing angle shall be no more than 2 degrees.



9 . HANDLING, SAFETY AND ENVIROMENTAL REQUIREMENTS

WARNING
The display module should be kept flat or fixed to a rigid, curved support with limited bending along the long axis. It should not be used for continual flexing and bending. Handle with care. Should the display break do not touch any material that leaks out. In case of contact with the leaked material then wash with water and soap.

CAUTION
The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.
Disassembling the display module can cause permanent damage and invalidate the warranty agreements.
IPA solvent can only be applied on active area and the back of a glass. For the rest part, it is not allowed.
Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged . Moreover the display is sensitive to static electricity and other rough environmental conditions.

Mounting Precautions
(1) It`s recommended that you consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the module.
(2) It`s recommended that you attach a transparent protective plate to the surface in order to protect the EPD. Transparent protective plate should have sufficient strength in order to resist external force.
(3) You should adopt radiation structure to satisfy the temperature specification.
(4) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the PS at high temperature and the latter causes circuit break by electro-chemical reaction.
(5) Do not touch, push or rub the exposed PS with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment. Do not touch the surface of PS for bare hand or greasy cloth. (Some cosmetics deteriorate the PS)
(6) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach the PS. Do not use acetone, toluene and alcohol because they cause chemical damage to the PS.
(7) Wipe off saliva or water drops as soon as possible. Their long time contact with PS causes deformations and color fading.

Data sheet status	
Product specification	The data sheet contains final product specifications.

Limiting values

Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information

Where application information is given, it is advisory and dose not form part of the specification.

Product Environmental certification

ROHS

REMARK

All The specifications listed in this document are guaranteed for module only. Post-assembled operation or component(s) may impact module performance or cause unexpected effect or damage and therefore listed specifications is not warranted after any Post-assembled operation.

10. Reliability test

10.1 Reliability Test Items

	TEST	CONDITION	REMARK
1	High-Temperature Operation	T=50℃, RH=30%RH, for 240Hr	
2	Low-Temperature Operation	T = 0℃, RH=30%RH for 240 hrs	
3	High-Temperature Storage	T=70℃ RH=40%RH For 240Hr	Test in white pattern
4	Low-Temperature Storage	T = -25℃ for 240 hrs	Test in white pattern
5	High Temperature, High-Humidity Operation	T=40℃,RH=90%RH,For 168Hr	
6	High Temperature, High- Humidity Storage	T=60℃,RH=80%RH,For 168Hr	Test in white pattern
7	Temperature Cycle	-25℃(30min)~70℃(30min),100 Cycle	Test in white pattern
8	Package Vibration	1.04G,Frequency : 20~200Hz Direction : X,Y,Z Duration: 30 minutes in each direction	Full packed for shipment
9	Package Drop Impact	Drop from height of 100 cm on Concrete surface Drop sequence:1 corner, 3edges, 6face One drop for each.	Full packed for shipment
10	Electrostatic discharge(non-operating)	Machine model: +/-250V,0Ω,200pF	

Actual EMC level to be measured on customer application.

Note1：Stay white pattern for storage and non-operation test.

Note2：In the standard conditions, there is not display function NG issue occurred. (including : line defect ,no image). All the cosmetic specification is judged before the reliability stress.

Note3：Keep testing after 2 hours placing at 20℃-25℃

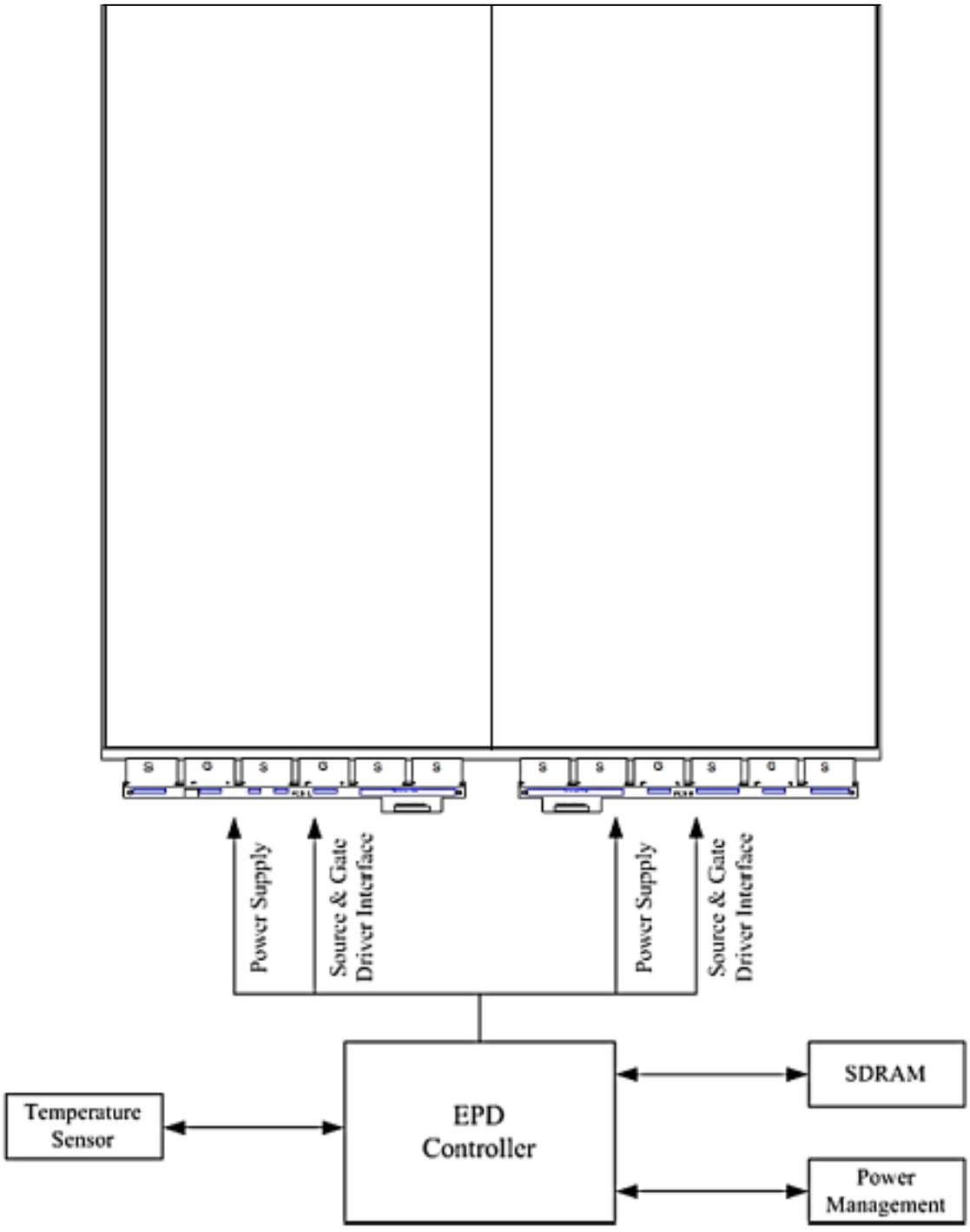
Note4: The protective film must be removed before temperature test.

10.2 Product warranty

Warranty conditions have to be negotiated between Xingtai and individual customers.

Xingtai provides 12+1(one month delivery time) months warranty for all products which are purchased from Xingtai.

11.Block Diagram



12. Packing

TBD