Specification For HINK 31.2''EPD

Model NO.: HINK-E312A02

Product VER:A0

Customer Approval

Customer	
Approval By	
Date Of Approval	

It will be agreed by the receiver,if not sign back the Specification within 15days.

Prepared By	Checked By	Approval By
Daisy Zhu	Yufeng Zhou	Ziping Hu

Version	Content	Date	Producer
A0	New release	2022/03/03	Daisy Zhu

CONTENTS

1. General Description

E312A02 is a reflective electrophoretic E Ink® technology display module based on active matrix TFT substrate. It has 31.2" active area with 2560 x 1440 pixels, the display is capable to display images at 2 to 16 gray levels (1 to 4 bits) depending on the display controller and the associated waveform file it used.

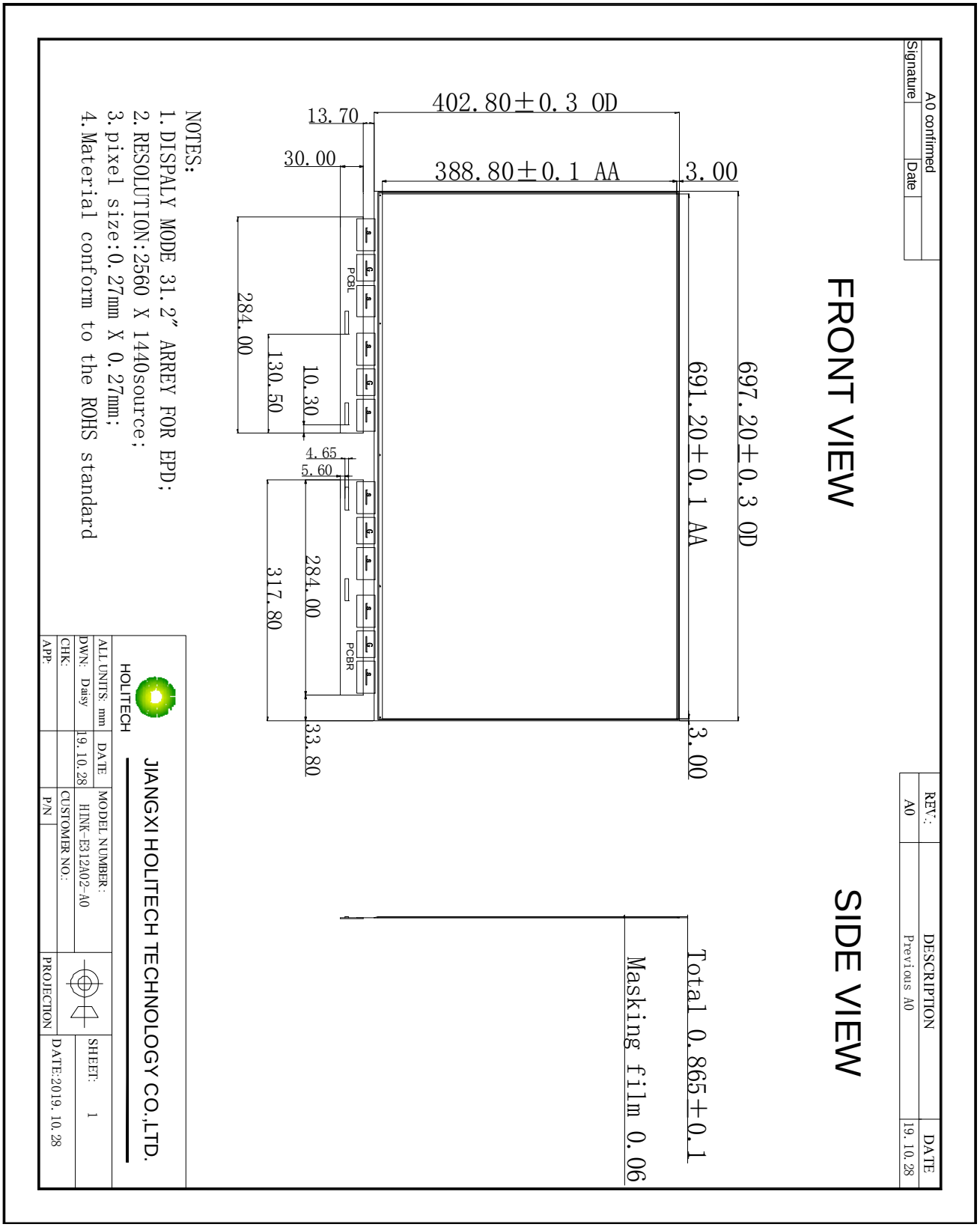
2.Features

- 2560 x 1440 resolution
- High contrast
- High reflectance
- Ultra wide viewing angle
- Ultra low power consumption
- Pure reflective mode
- Image stable
- Landscape/Portrait mode
- Bi-stable display
- Commercial temperature range
- Landscape mode

3. Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	31.2	Inch	
Display Resolution	2560 (H) × 1440 (V)	Pixel	7:4
Active Area	691.2 (H) × 388.8 (V)	mm	
Pixel Pitch	0.27 (H) × 0.27 (V)	mm	
Pixel Configuration	Rectangle		
Outline Dimension	697.2(H) × 402.8(V) × 0.805(D)	mm	w/o masking film
Module Weight	494±20	g	
Display operating mode	Reflective mode		
Surface treatment	Anti-glare		

4. Mechanical Drawing of EPD module



5 Input/Output Terminals

5-1)Connector type：P-TWO 196033-50041 compatible

5-2)Pin Assignment

Connector L2

Pin #	Signal	Description
1	VGL	Negative power supply gate driver
2	NC	NO Connection
3	VGH	Positive power supply gate driver
4	Mode2	Output mode selection gate driver
5	VDD	Digital power supply drivers
6	Mode1	Output mode selection gate driver
7	CKV	Clock gate driver
8	STV	Start pulse gate driver
9	VSS	Ground
10	VCOM_TFT	Common voltage
11	VDD	Digital power supply drivers
12	VSS	Ground
13	XCL	Clock source driver
14	D0	Data signal source driver
15	D1	Data signal source driver
16	D2	Data signal source driver
17	D3	Data signal source driver
18	D4	Data signal source driver
19	D5	Data signal source driver
20	D6	Data signal source driver
21	D7	Data signal source driver
22	VSS	Ground
23	D8	Data signal source driver
24	D9	Data signal source driver
25	D10	Data signal source driver
26	D11	Data signal source driver
27	D12	Data signal source driver
28	D13	Data signal source driver
29	D14	Data signal source driver
30	D15	Data signal source driver
31	XSTL	Start pulse source driver
32	XLE	Latch enable source driver
33	XOE	Output enable source driver
34	ISEL	L: input data bus width is 8-bit, i.e., D7 ~ D0 are valid
35	NC	NO Connection
36	VPOS	Positive power supply source driver
37	NC	NO Connection
38	VNEG	Negative power supply source driver
39	VCOM_FPL	Common Voltage
40	NC	NO Connection
41	STV2	Start pulse gate driver 2
42	G640	Detect IC function
43	S400	Detect IC function
44	S320	Detect IC function
45	NC	NO Connection
46	G640	Detect IC function
47	S400	Detect IC function
48	S320	Detect IC function
49	NC	NO Connection
50	STL2	Data shift start pulse 2

Connector L1

Pin #	Signal	Description
1	VGL	Negative power supply gate driver
2	NC	NO Connection
3	VGH	Positive power supply gate driver
4	Mode2	Output mode selection gate driver
5	VDD	Digital power supply drivers
6	Mode1	Output mode selection gate driver
7	CKV	Clock gate driver
8	STV	Start pulse gate driver
9	VSS	Ground
10	VCOM_TFT	Common voltage
11	VDD	Digital power supply drivers
12	VSS	Ground
13	XCL	Clock source driver
14	D0	Data signal source driver
15	D1	Data signal source driver
16	D2	Data signal source driver
17	D3	Data signal source driver
18	D4	Data signal source driver
19	D5	Data signal source driver
20	D6	Data signal source driver
21	D7	Data signal source driver
22	VSS	Ground
23	D8	Data signal source driver
24	D9	Data signal source driver
25	D10	Data signal source driver
26	D11	Data signal source driver
27	D12	Data signal source driver
28	D13	Data signal source driver
29	D14	Data signal source driver
30	D15	Data signal source driver
31	XSTL	Start pulse source driver
32	XLE	Latch enable source driver
33	XOE	Output enable source driver
34	ISEL	L: input data bus width is 8-bit, i.e., D7 ~ D0 are valid
35	NC	NO Connection
36	VPOS	Positive power supply source driver
37	NC	NO Connection
38	VNEG	Negative power supply source driver
39	VCOM_FPL	Common Voltage
40	NC	NO Connection
41	STV2	Start pulse gate driver 2
42	NC	NO Connection
43	NC	NO Connection
44	NC	NO Connection
45	NC	NO Connection
46	NC	NO Connection
47	NC	NO Connection
48	NC	NO Connection
49	NC	NO Connection
50	STL2	Data shift start pulse 2

Connector R1

Pin #	Signal	Description
1	VGL	Negative power supply gate driver
2	NC	NO Connection
3	VGH	Positive power supply gate driver
4	Mode2	Output mode selection gate driver
5	VDD	Digital power supply drivers
6	Mode1	Output mode selection gate driver
7	CKV	Clock gate driver
8	STV	Start pulse gate driver
9	VSS	Ground
10	VCOM_TFT	Common voltage
11	VDD	Digital power supply drivers
12	VSS	Ground
13	XCL	Clock source driver
14	D0	Data signal source driver
15	D1	Data signal source driver
16	D2	Data signal source driver
17	D3	Data signal source driver
18	D4	Data signal source driver
19	D5	Data signal source driver
20	D6	Data signal source driver
21	D7	Data signal source driver
22	VSS	Ground
23	D8	Data signal source driver
24	D9	Data signal source driver
25	D10	Data signal source driver
26	D11	Data signal source driver
27	D12	Data signal source driver
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30	D15	Data signal source driver
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36	VPOS	Positive power supply source driver
37	NC	NO Connection
38	VNEG	Negative power supply source driver
39	VCOM_FPL	Common Voltage
40	NC	NO Connection
41	STV2	Start pulse gate driver 2
42	NC	NO Connection
43	NC	NO Connection
44	NC	NO Connection
45	NC	NO Connection
46	NC	NO Connection
47	NC	NO Connection
48	NC	NO Connection
49	NC	NO Connection
50	STL2	Data shift start pulse 2

Connector R2

Pin #	Signal	Description
1	VGL	Negative power supply gate driver
2	NC	NO Connection
3	VGH	Positive power supply gate driver
4	Mode2	Output mode selection gate driver
5	VDD	Digital power supply drivers
6	Mode1	Output mode selection gate driver
7	CKV	Clock gate driver
8	STV	Start pulse gate driver
9	VSS	Ground
10	VCOM_TFT	Common voltage
11	VDD	Digital power supply drivers
12	VSS	Ground
13	XCL	Clock source driver
14	D0	Data signal source driver
15	D1	Data signal source driver
16	D2	Data signal source driver
17	D3	Data signal source driver
18	D4	Data signal source driver
19	D5	Data signal source driver
20	D6	Data signal source driver
21	D7	Data signal source driver
22	VSS	Ground
23	D8	Data signal source driver
24	D9	Data signal source driver
25	D10	Data signal source driver
26	D11	Data signal source driver
27	D12	Data signal source driver
28	D13	Data signal source driver
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30	D15	Data signal source driver
31	XSTL	Start pulse source driver
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36	VPOS	Positive power supply source driver
37	NC	NO Connection
38	VNEG	Negative power supply source driver
39	VCOM_FPL	Common Voltage
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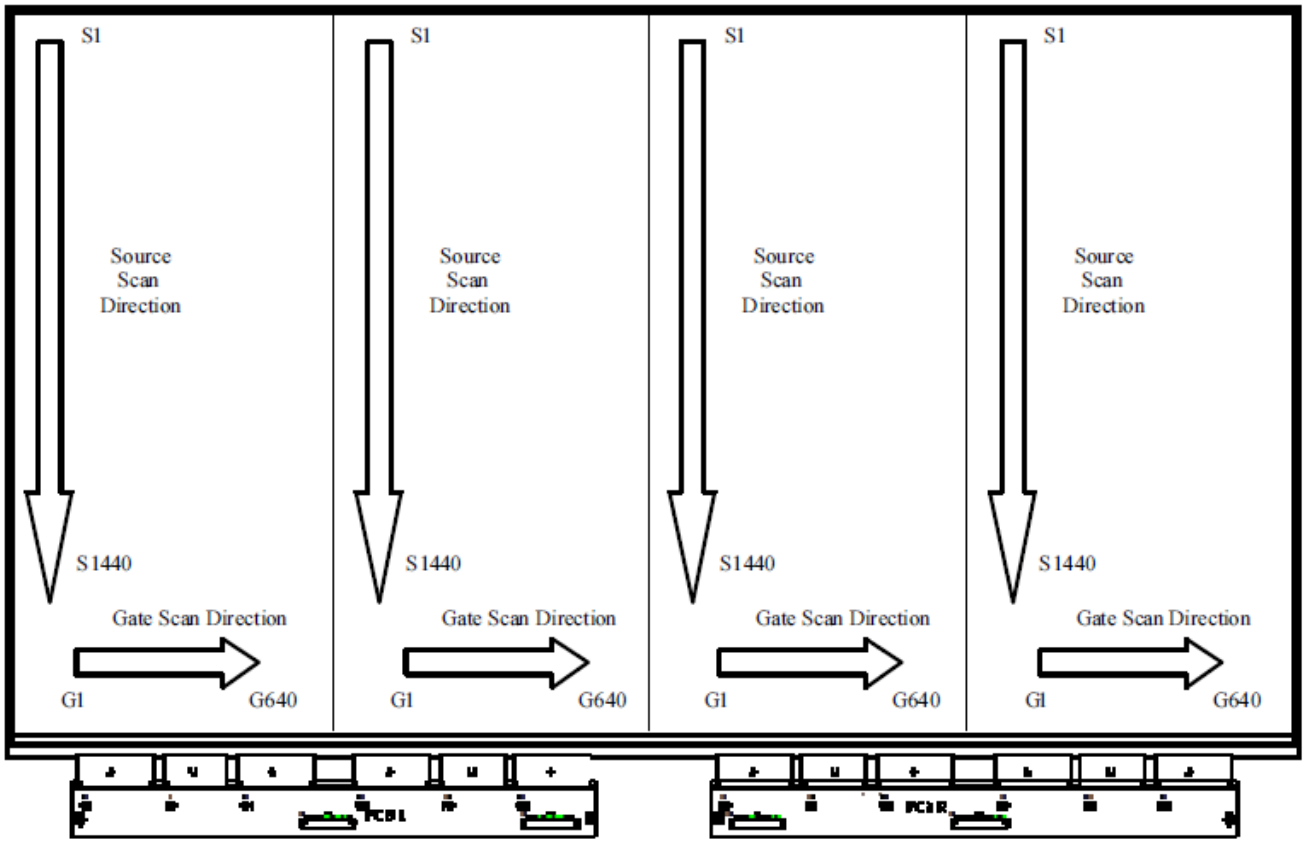
42	G640	Detect IC function
43	S400	Detect IC function
44	S320	Detect IC function
45	NC	NO Connection
46	NC	NO Connection
47	S320	Detect IC function
48	S400	Detect IC function
49	G640	Detect IC function
50	STL2	Data shift start pulse 2

5-3) Panel Scan direction



6. Display Module Electrical Characteristics

6.1 Absolute maximum rating

Parameter	Symbol	Rating	Unit	Remark
Logic Supply Voltage	VDD	-0.3 to +7	V	--
Positive Supply Voltage	V_{POS}	-0.3 to +18	V	--
Negative Supply Voltage	V_{NEG}	+0.3 to -18	V	--
Max .Drive Voltage Range	V_{POS} - V_{NEG}	36	V	--
Supply Voltage	VGH	-0.3 to +55	V	--
Supply Voltage	VGL	-32 to +0.3	V	--
Supply Range	VGH-VGL	-0.3 to +55	V	--
Operating Temp. Range	TOTR	0 to +50	℃	--
Storage Temperature	TSTG	-25 to +70	℃	--

6.2 Panel DC characteristics

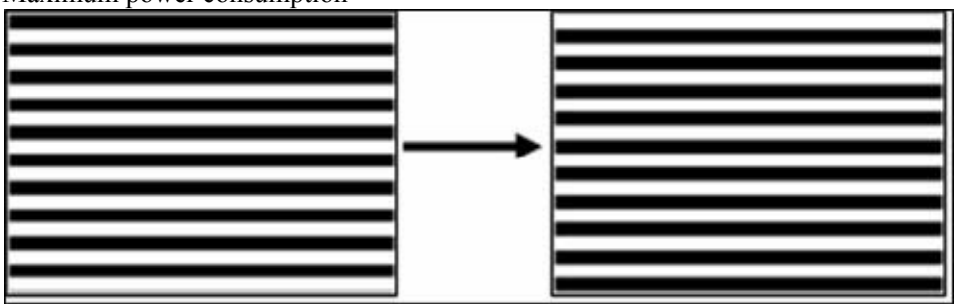
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Signal ground	V_{SS}		-	0	-	V
Logic Voltage supply	V_{DD}		2.7	3.3	3.6	V
	I_{VDD}	V_{DD}= 3.3V	-	3	7	mA
Gate Negative supply	V_{GL}		-21	-20	-19	V
	I_{GL}	V_{GL} = -20V	-	4	9	mA
Gate Positive supply	V_{GH}		21	22	23	V
	I_{GH}	V_{GH} = 22V	-	3	6	mA
Source Negative supply	V_{NEG}		-15.4	-15	-14.6	V
	I_{NEG}	V_{NEG} = -15V	-	7	415	mA
Source Positive supply	V_{POS}		14.6	15	15.4	V
	I_{POS}	V_{POS} = 15V	-	7	445	mA
Asymmetry source	V_{Asym}	V_{POS}+V_{NEG}	-800	-	+800	mV
Common voltage	V_{COM}		-2.96	Adjusted	-2.04	V
	I_{COM}		-	1.2	-	mA
Panel power	P		-	370	13300	mW
Standby power panel	P_{STBY}		-	-	1.32	mW

- The maximum power consumption is measured using 50Hz waveform with following pattern transition: from pattern of repeated 1 consecutive black scan lines followed by 1 consecutive white scan line to that of repeated 1 consecutive white scan lines followed by 1 consecutive black scan lines. (Note 6-1)

- The Typical power consumption is measured using 50Hz waveform with following pattern transition: from horizontal 4 gray scale pattern to vertical 4 gray scale pattern. (Note 6-2)
- The standby power is the consumed power when the panel controller is in standbymode.
- The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by E Ink.
- Vcom is recommended to be set in the range of assigned value ± 0.1V.
- The maximum I_{COM} inrush current is about 2 A

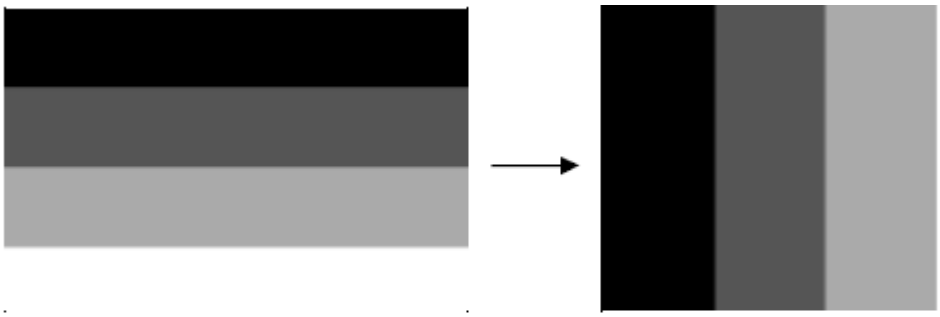
Note 6-1

The Maximum power consumption



Note 6-2

The Typical power consumption



6-3)Refresh Rate

The module E312A02 is applied at a maximum screen refresh rate of 50Hz.

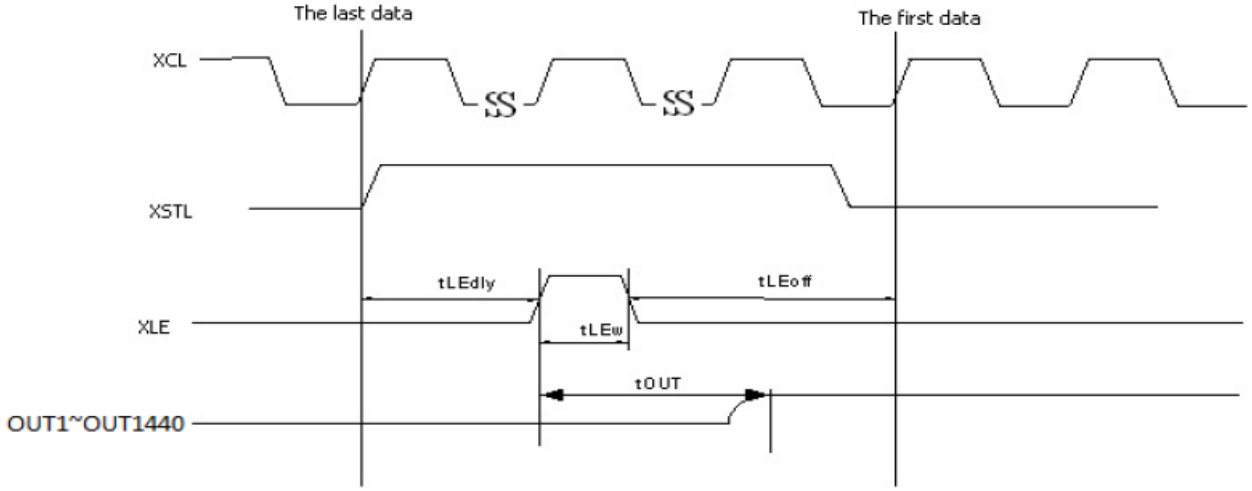
	Min	Max
Refresh Rate	-	50Hz

6-4)Panel AC characteristics

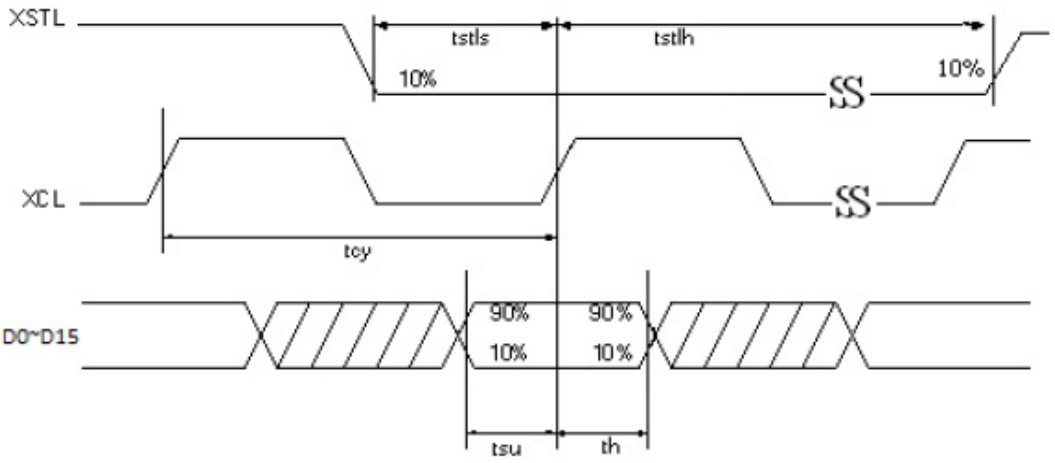
VDD=2.7 V to 3.6V, unless otherwise specified.

Para meter	Symbol	Min.	Typ.	Max.	Unit
Clock frequency	fckv	-	-	200	kHz
Minimum “L” clock pulse width	twL	0.5	-	-	us
Minimum “H” clock pulse width	twH	0.5	-	-	us
Clock rise time	trckv	-	-	100	ns
Clock fall time	tfckv	-	-	100	ns
SPV setup time	tSU	100	-	twH-100	ns
SPV hold time	tH	100	-	twH-100	ns
Pulse rise time	trspv	-	-	100	ns
Pulse fall time	tfspv	-	-	100	ns
Clock XCL cycle time	tcy	16.7	20	-	ns
D0 .. D7 setup time	tsu	8	-	-	ns
D0 .. D7 hold time	th	8	-	-	ns
XSTL setup time	tstls	8	-	-	ns
XSTL hold time	tstlh	8	-	-	ns
XLE on delay time	tLEdly	40	-	-	ns
XLE high-level pulse width (When VDD=2.7V to 3.6V)	tLEw	40	-	-	ns
XLE off delay time	tLEoff	200	-	-	ns
Output setting time to +/- 30mV(C_{load}=200pF)	tout	-	-	12	us

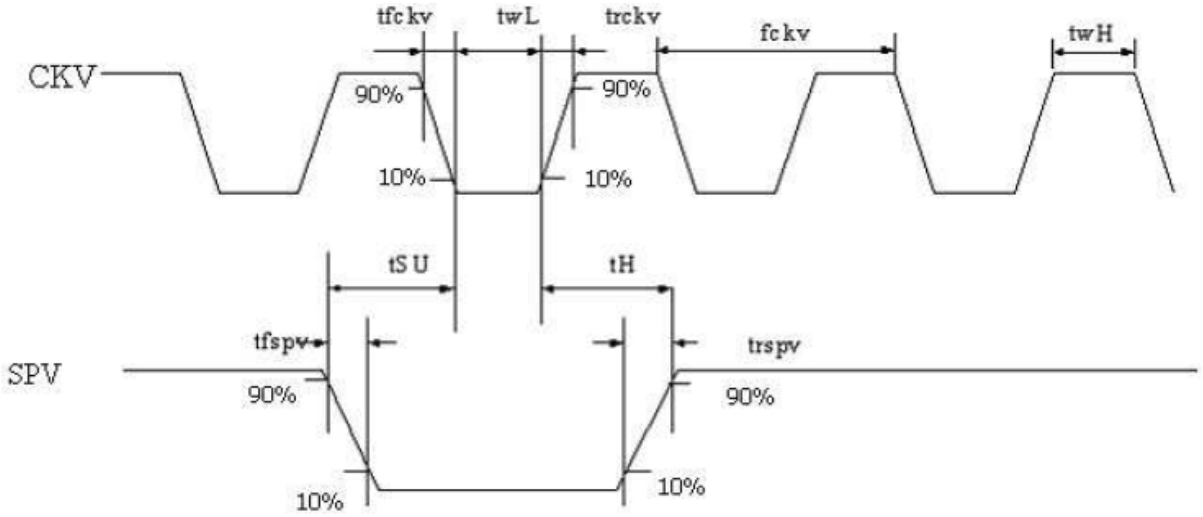
OUTPUT LATCH CONTROL SIGNALS



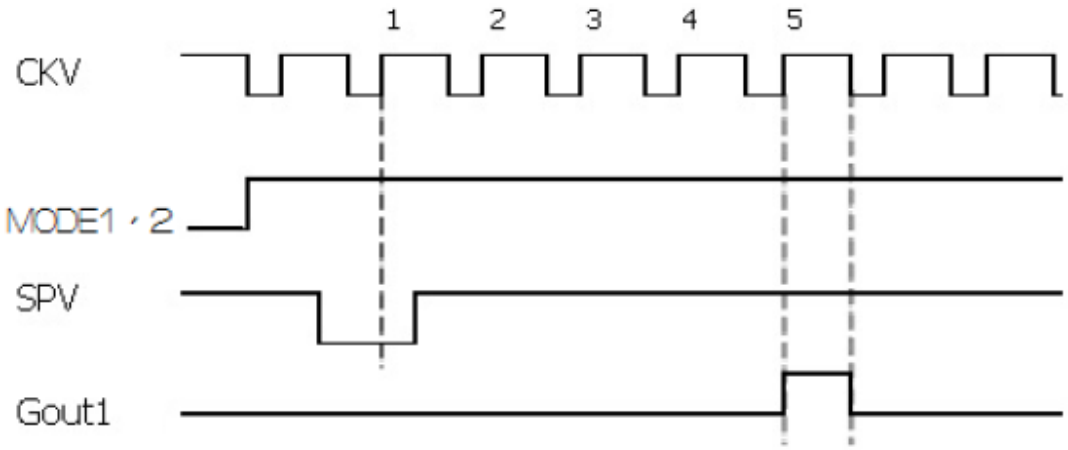
CLOCK & DATA TIMING



CKV & SPV TIMING



GATE OUTPUT TIMING



Note：First gate line on timing

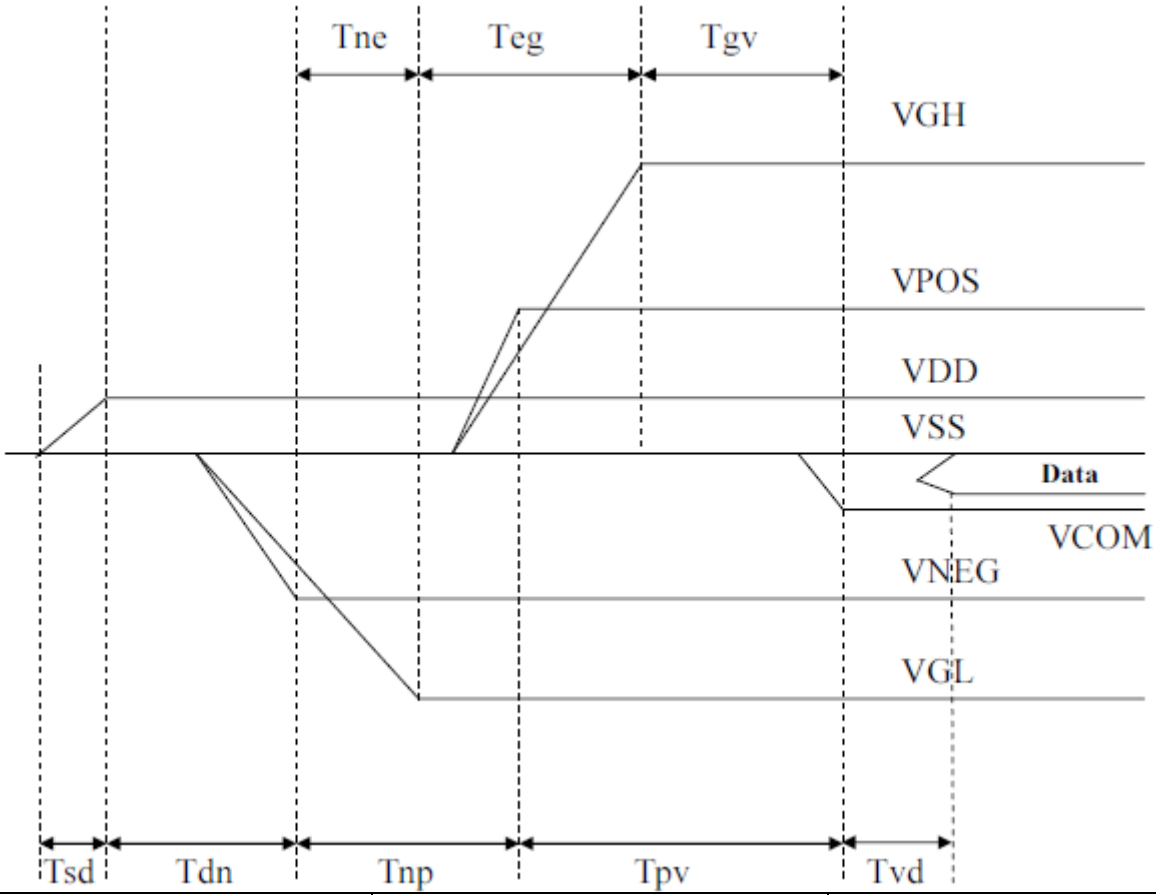
After 5CKV，gate line is on .

7.Power Sequence

Power Rails must be sequenced in the following order：

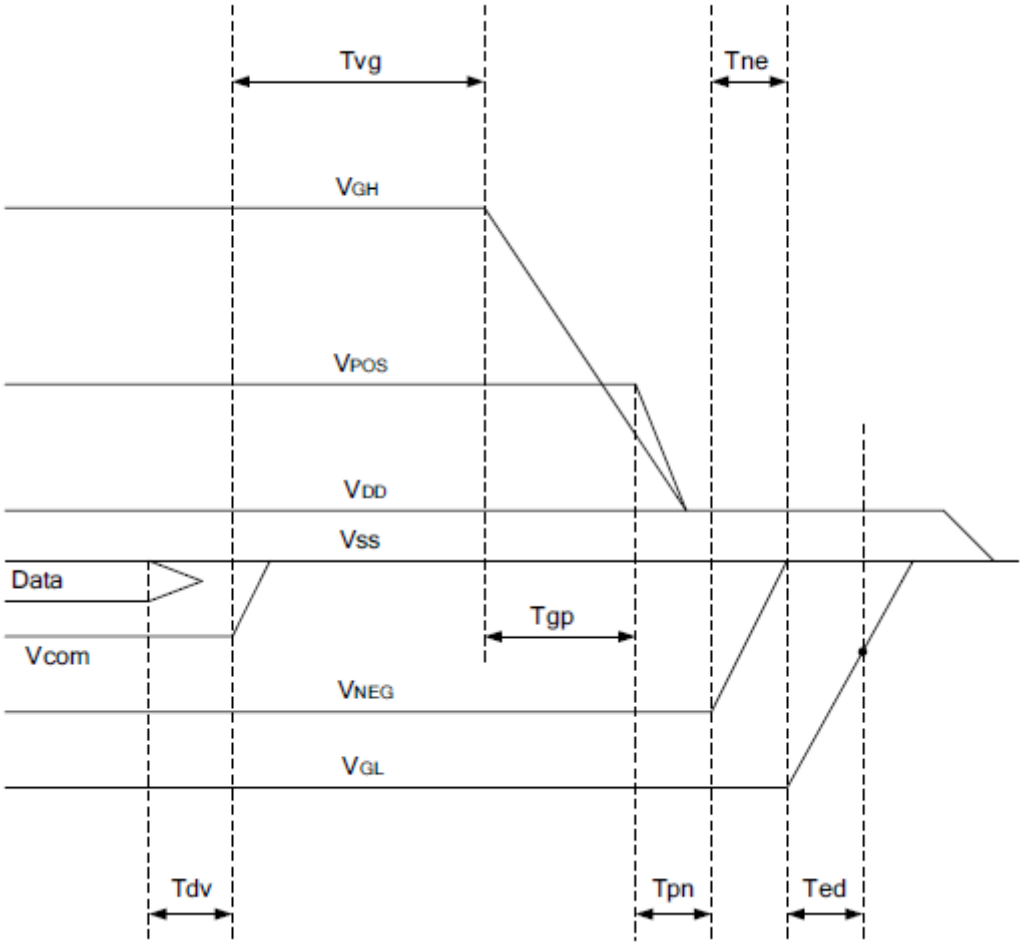
1. VSS → VDD →VN3 →VNEG→ VPOS（Source driver） → VCOM
2. VSS →VDD → VGL → VGH (Gate driver)

POWER ON



	Min	Max
Tsd	30us	-
Tde	100us	-
Tep	1000us	-
Tpv	100us	-
Tvd	100us	-
Ten	0us	-
Tng	1000us	-
Tgv	100us	-

POWER OFF



	Min	Max	Remark
Tdv	100μs	-	-
Tvg	0μs	-	-
Tgp	0μs	-	-
Tpn	0μs	-	-
Tne	0μs	-	-
Ted	0.5s	-	Discharged point @ -7.4 Volt

Note1： Supply voltages decay through pull-down resistors.
Note2： Begin to turn off VGL power after VNEG and VPOS are completely or almost discharged to GND state.
Note3： VGL must remain negative of Vcom during decay period

8. Optical characteristics

8.1 Specification

Measurements are made with that the illumination is under an angle of 45 degrees, the detector is perpendicular unless otherwise specified.

T=25±2℃

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT	Note
R	Reflectance	White	30	40	--	%	--
Gn	Nth Grey level	-	-	DS+(WS-DS)×n(m-1）	-	L*	--
CR	Contrast Ratio	-	10	12	-		--

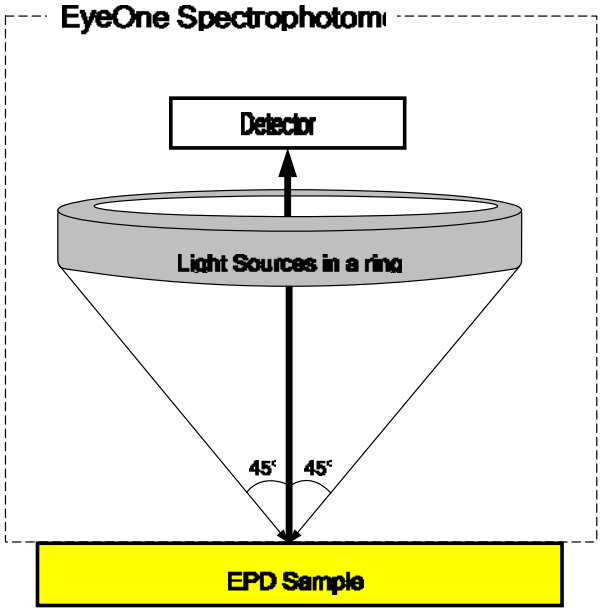
WS: White state , DS: Dark state, Gray state from Dark to White :DS、G1、G2…、Gn…、Gm-2、WSm:4、8、16 when 2、3、4 bits mode

Note 8-1：Luminance meter：Eye – One Pro Spectrophotometer

8. 2 Definition of contrast ratio

The contrast ratio (CR) is the ratio between the reflectance in a full white area (Rl) and the reflectance in a dark area (Rd):

CR = Rl/Rd

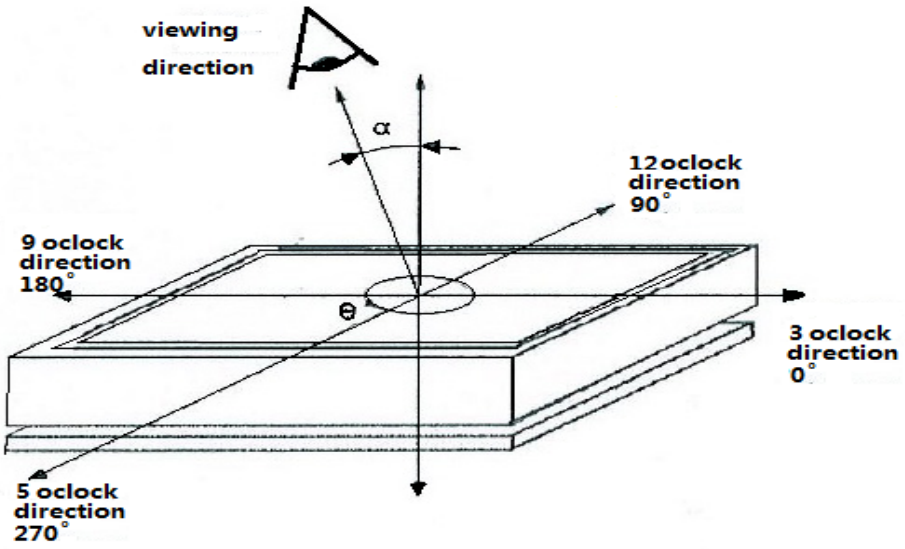


8. 3 Reflection Ratio

The reflection ratio is expressed as:

R = Reflectance Factor $_{\text{white board}}$ x (L_{center} / $L_{\text{white board}}$)

L_{center} is the luminance measured at center in a white area (R=G =B=1). $L_{\text{white board}}$ is the luminance of a standard white board. Both are measured with equivalent illumination source. The viewing angle shall be no more than 2 degrees.



9 . HANDLING, SAFETY AND ENVIROMENTAL REQUIREMENTS

WARNING
The display module should be kept flat or fixed to a rigid, curved support with limited bending along the long axis. It should not be used for continual flexing and bending. Handle with care. Should the display break do not touch any material that leaks out. In case of contact with the leaked material then wash with water and soap.

CAUTION
The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.
Disassembling the display module can cause permanent damage and invalidate the warranty agreements.
IPA solvent can only be applied on active area and the back of a glass. For the rest part, it is not allowed.
Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged . Moreover the display is sensitive to static electricity and other rough environmental conditions.

Mounting Precautions
(1) It`s recommended that you consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the module.
(2) It`s recommended that you attach a transparent protective plate to the surface in order to protect the EPD. Transparent protective plate should have sufficient strength in order to resist external force.
(3) You should adopt radiation structure to satisfy the temperature specification.
(4) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the PS at high temperature and the latter causes circuit break by electro-chemical reaction.
(5) Do not touch, push or rub the exposed PS with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment. Do not touch the surface of PS for bare hand or greasy cloth. (Some cosmetics deteriorate the PS)
(6) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach the PS. Do not use acetone, toluene and alcohol because they cause chemical damage to the PS.
(7) Wipe off saliva or water drops as soon as possible. Their long time contact with PS causes deformations and color fading.

Data sheet status	
Product specification	The data sheet contains final product specifications.

Limiting values

Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information

Where application information is given, it is advisory and dose not form part of the specification.

Product Environmental certification

ROHS

REMARK

All The specifications listed in this document are guaranteed for module only. Post-assembled operation or component(s) may impact module performance or cause unexpected effect or damage and therefore listed specifications is not warranted after any Post-assembled operation.

10. Reliability test

10.1 Reliability Test Items

	TEST	CONDITION	REMARK
1	High-Temperature Operation	T=50℃, RH=30%RH, for 240Hr	
2	Low-Temperature Operation	T = 0℃, RH=30%RH for 240 hrs	
3	High-Temperature Storage	T=70℃ RH=23%RH For 240Hr	Test in white pattern
4	Low-Temperature Storage	T = -25℃ for 240 hrs	Test in white pattern
5	High Temperature, High-Humidity Operation	T=40℃,RH=90%RH,For 168Hr	
6	High Temperature, High- Humidity Storage	T=60℃,RH=80%RH,For 168Hr	Test in white pattern
7	Temperature Cycle	-25℃(30min)~70℃(30min),100 Cycle	Test in white pattern
8	Package Vibration	1.04G,Frequency : 20~200Hz Direction : X,Y,Z Duration: 30 minutes in each direction	Full packed for shipment
9	Package Drop Impact	Drop from height of 100 cm on Concrete surface Drop sequence:1 corner, 3edges, 6face One drop for each.	Full packed for shipment
10	Electrostatic discharge(non-operating)	Machine model: +/-250V,0Ω,200pF	

Actual EMC level to be measured on customer application.

Note1：Stay white pattern for storage and non-operation test.

Note2：In the standard conditions, there is not display function NG issue occurred. (including : line defect ,no image). All the cosmetic specification is judged before the reliability stress.

Note3：Keep testing after 2 hours placing at 20℃-25℃

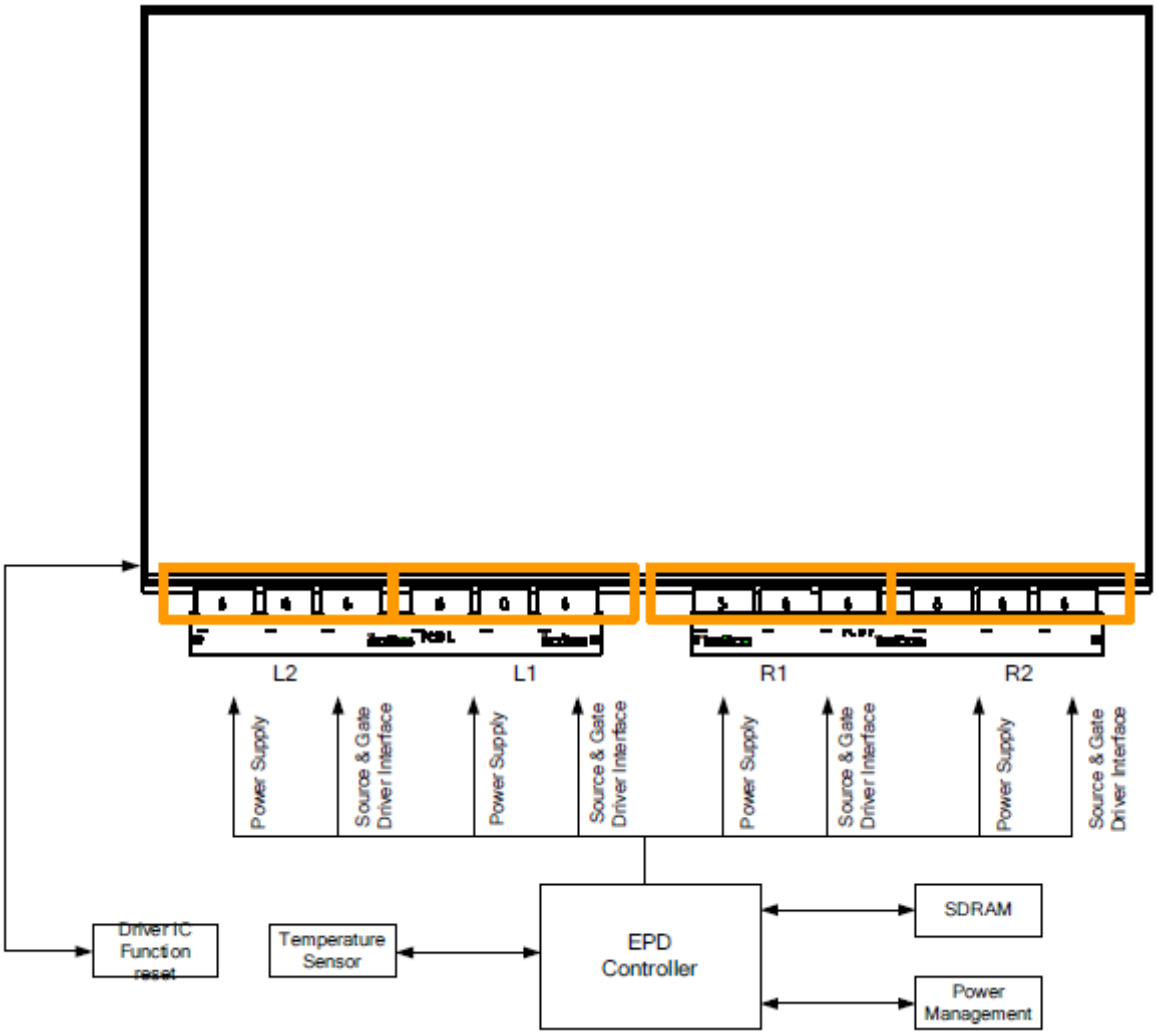
Note4: The protective film must be removed before temperature test.

10.2 Product warranty

Warranty conditions have to be negotiated between Xingtai and individual customers.

Xingtai provides 12+1(one month delivery time) months warranty for all products which are purchased from Xingtai.

11.Block Diagram



12. Packing

TBD