



File Name	Specification For HINK 4.2" EPD	Module Number	HINK-E042A88
Version	A0	Page Number	1 of 37

Specification For HINK4.2"EPD

Model NO.: HINK-E042A88

Product VER:A0

Customer Approval

Customer	
Approval By	
Date Of Approval	

It will be agreed by the receiver,if not sign back the Specification within 15days.

Prepared By	Checked By	Approval By
Daisy Zhu	Zhou Yufeng	Hu Ziping



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Version	Content	Date	Producer
A0	New release	2020/11/03	Daisy Zhu



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1. GENERAL DESCRIPTION

HINK-E042A88 is an Active Matrix Electrophoretic Display (AMEPD), with interface and a reference system design. The 4.2" active area contains 400×300 pixels, and has 1-bit B/W/R full display capabilities. An integrated circuit contains gate buffer, source buffer, interface, timing control logic, oscillator, DC-DC, SRAM, LUT, VCOM and border are supplied with each panel.

2. FEATURES

- 400×300 pixels display
- High contrast
- High reflectance
- Ultra wide viewing angle
- Ultra low power consumption
- Pure reflective mode
- Bi-stable display
- Commercial temperature range
- Landscape, portrait modes
- Hard-coat antiglare display surface
- Ultra Low current deep sleep mode
- On chip display RAM
- Low voltage detect for supply voltage
- High voltage ready detect for driving voltage
- Internal temperature sensor
- 10-byte OTP space for module identification
- Serial peripheral interface available
- On-chip oscillator
- On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage
- I2C signal master interface to read external temperature sensor/ built-in temperature sensor

3. APPLICATION

Electronic Shelf Label System

4. MECHANICAL SPECIFICATIONS

Parameter	Specifications	Unit	Remark
Screen Size	4.2	Inch	
Display Resolution	400(H)×300(V)	Pixel	Dpi:119
Active Area	84.8(H)×63.6 (V)	mm	
Pixel Pitch	0.212×0.212	mm	
Pixel Configuration	Square		
Outline Dimension	91.00(H)× 77.00(V) × 1.1(D)	mm	Without masking film
Weight	15±0.5	g	



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5. MECHANICAL DRAWING OF EPD MODULE

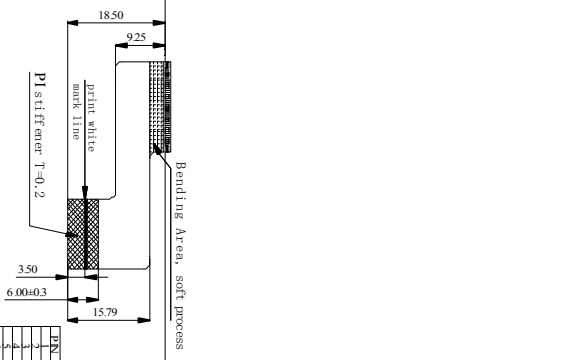
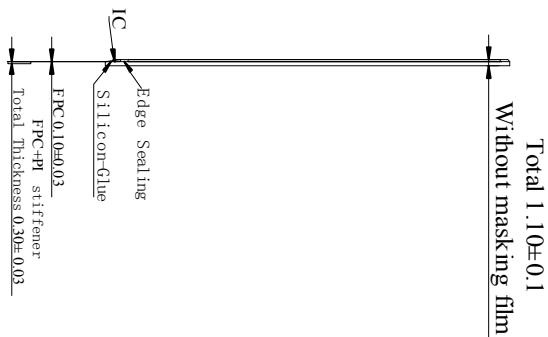
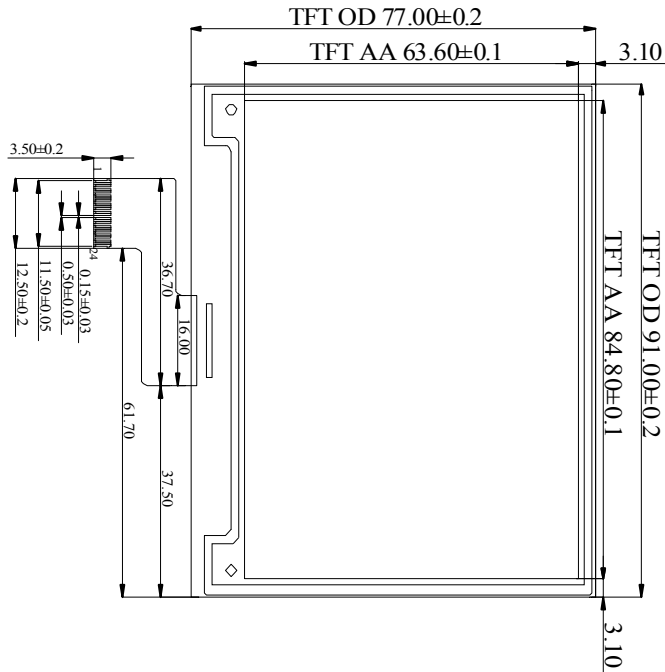
A0 confirmed	
Signature	Date

FRONT VIEW

SIDE VIEW

BOTTOM VIEW

REV.:	DESCRIPTION	DATE
A0	Previous A0	2020.10.26



PN	SKETCH
1	SK
2	DR
3	RISH
4	NS
5	NS12
6	NSA
7	NSA
8	ELSS
9	ELSS
10	ELSS
11	DCV
12	DCV
13	SN
14	VDDO
15	VDDO
16	VDDO
17	VDDO
18	VDDO
19	VDDO
20	VDDO
21	VDDO
22	VDDO
23	VDDO
24	VDDO

- NOTES:
- 1.DISPALY MODE 4.2 ARREY FOR EPD;
 - 2.DRIVE IC: SSD1683
 - 3.RESOLUTION:300gate X 400s ounce;
 - 4.pixel pitch:0.212mm X 0.212mm;
 - 5.dpi:120
 - 6.Unspecified Tolerance:±0.20;
 - 7.Material conform to the ROHS standar

		JIANGXI HOLITECH TECHNOLOGY CO.,LTD.	
ALL UNITS: mm	DATE	MODEL NUMBER:	
D.V.N: June	2020.10.26	HINK-B042A88-A0	
CHK:		CUSTOMER NO	
App:		PN	
		SHEET: 1	
		DATE: 2020.10.26	



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6. INPUT/OUTPUT TERMINALS

Pin #	Single	Description	Remark
1	NC	No connection and do not connect with other NC pins NC	Keep Open
2	GDR	N-Channel MOSFET Gate Drive Control	
3	RESE	Current Sense Input for the Control Loop	
4	NC	No connection and do not connect with other NC pins	Keep Open
5	VSH2	Positive Source driving voltage	
6	TSCL	I2C Interface to digital temperature sensor Clock pin	
7	TSDA	I2C Interface to digital temperature sensor Date pin	
8	BS1	Bus selection pin	Note 6-5
9	BUSY	Busy state output pin	Note 6-4
10	RES #	Reset	Note 6-3
11	D/C #	Data /Command control pin	Note 6-2
12	CS #	Chip Select input pin	Note 6-1
13	SCL	serial clock pin (SPI)	
14	SDA	serial data pin (SPI)	
15	VDDIO	Power for interface logic pins	
16	VCI	Power Supply pin for the chip	
17	VSS	Ground	
18	VDD	Core logic power pin	
19	VPP	Power Supply for OTP Programming	
20	VSH1	Positive Source driving voltage	
21	VGH	Power Supply pin for Positive Gate driving voltage and VSH	
22	VSL	Negative Source driving voltage	
23	VGL	Power Supply pin for Negative Gate driving voltage, VCOM and VSL	
24	VCOM	VCOM driving voltage	

Note 6-1: This pin (CS#) is the chip select input connecting to the MCU. The chip is enabled for MCU communication: only when CS# is pulled LOW.

Note 6-2: This pin (D/C#) is Data/Command control pin connecting to the MCU. When the pin is pulled HIGH, the data will be interpreted as data. When the pin is pulled set is active low.

Note 6-4: This pin (BUSY) is Busy state output pin. When Busy is High the operation of chip should not be interrupted and any commands should not be issued to the module. The driver IC will put Busy pin High when the driver IC is working such as:

- Outputting display waveform;
- Communicating with digital temperature sensor

Note 6-5: This pin (BS1) is for 3-line SPI or 4-line SPI selection. When it is “Low”, 4-line SPI is selected. When it is “High”, 3-line SPI (9 bits SPI) is selected.



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7. MCU INTERFACE

7.1 MCU Interface selection

The E042A88 can support 3-wire/4-wire serial peripheral. MCU interface is pin selectable by BS1 shown in Table7-1.

Note:

- (1) L is connected to VSS
- (2) H is connected to VDDIO

Table 7-1 : Interface pins assignment under different MCU interface

MCU Interface	Pin Name					
	BS1	RES#	CS#	D/C#	SCL	SDA
4-wire serial peripheral interface (SPI)	L	RES#	CS#	D/C#	SCL	SDA
3-wire serial peripheral interface (SPI) – 9 bits SPI	H	RES#	CS#	L	SCL	SDA

7.2 MCU Serial Interface (4-wire SPI)

The 4-wire SPI consists of serial clock SCL, serial data SDA, D/C# and CS#. The control pins status in 4-wire SPI in writing command/data is shown in Table 7-2 and the write procedure 4-wire SPI is shown in Table 7-2

Table 7-2 : Control pins status of 4-wire SPI

Function	SCL pin	SDA pin	D/C# pin	CS# pin
Write command	↑	Command bit	L	L
Write data	↑	Data bit	H	L

Note:

- (1) L is connected to VSS and H is connected to VDDIO
- (2) ↑ stands for rising edge of signal
- (3) SDA(Write Mode) is shifted into an 8-bit shift register on each rising edge of SCL in the order of D7, D6, ... D0. The level of D/C# should be kept over the whole byte. The data byte in the shift register is written to the Graphic Display Data RAM (RAM)/Data Byte register or command Byte register according to D/C# pin.

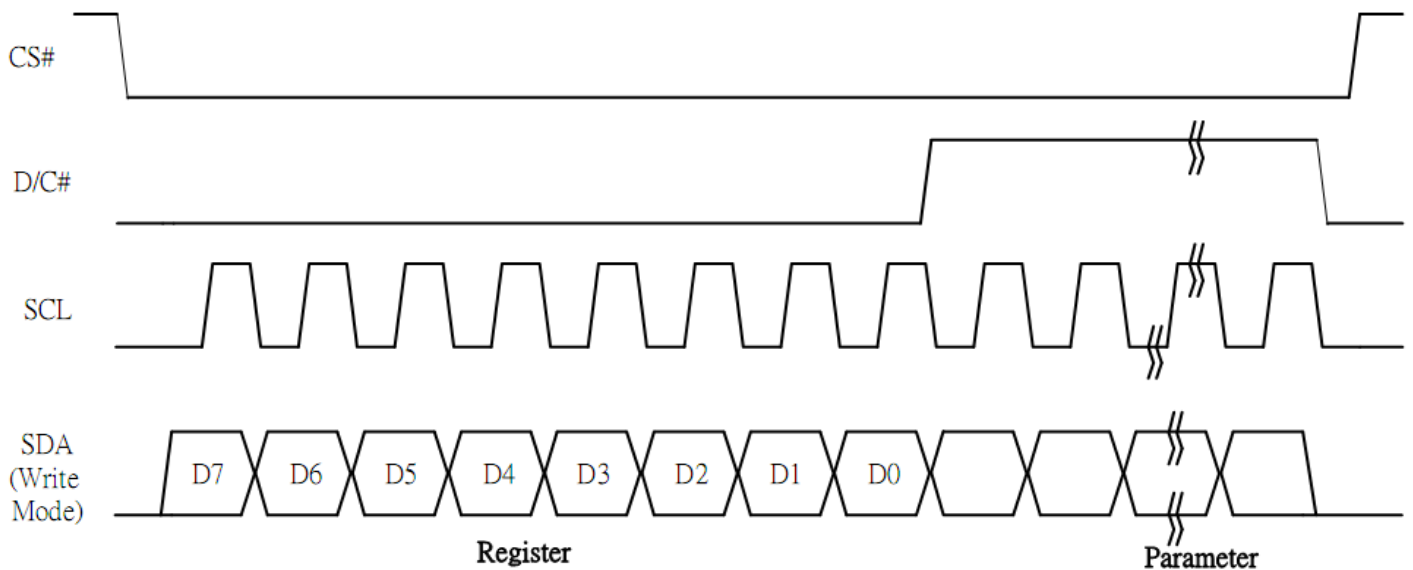
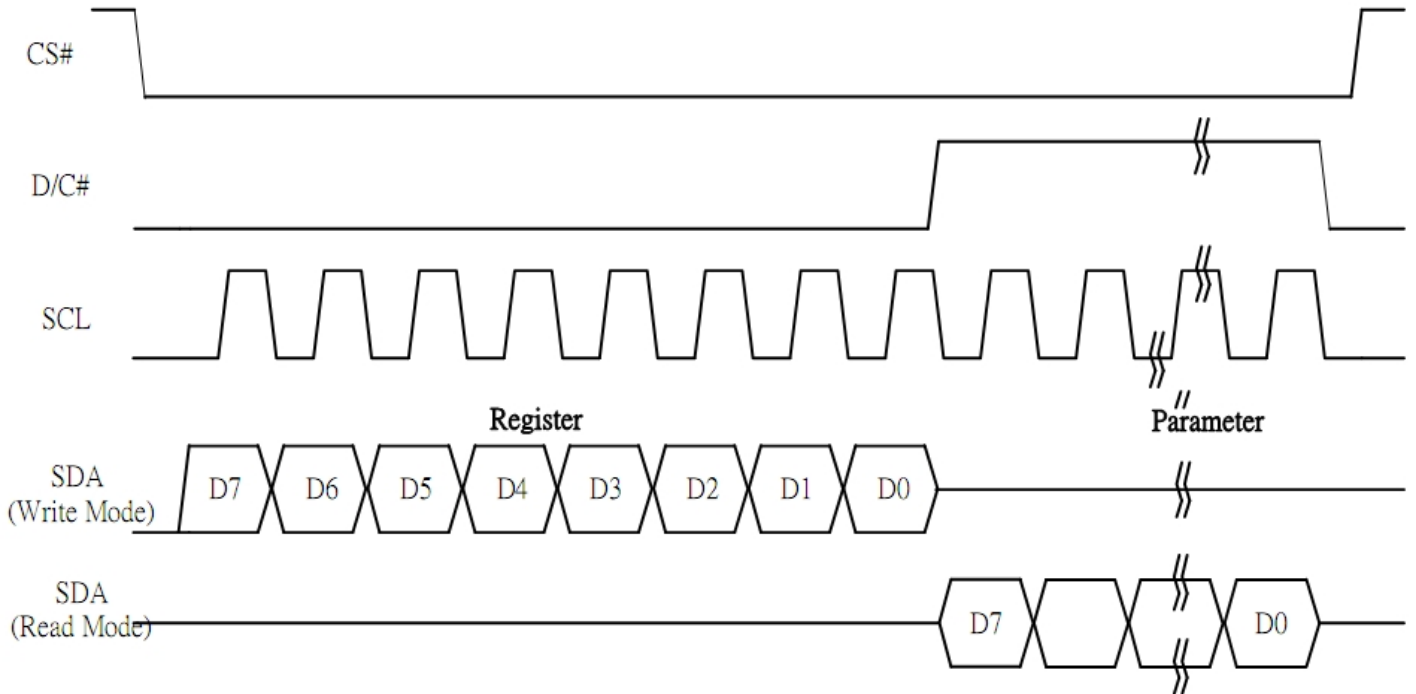


Figure 7-1 : Write procedure in 4-wire SPI mode

In the read operation (Command 0x1B, 0x27, 0x2D, 0x2E, 0x2F, 0x35). After CS# is pulled low, the first byte sent is command byte, D/C# is pulled low. After command byte sent, the following byte(s) read are data byte(s), so D/C# bit is then pulled high. An 8-bit data will be shifted out on every clock falling edge. The serial data SDA bit shifting sequence is D7, D6, to D0 bit. Figure 7-2 shows the read procedure in 4-wire SPI.



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7.3 MCU Serial Peripheral Interface (3-wire SPI)

The 3-wire SPI consists of serial clock SCL, serial data SDA and CS#. The operation is similar to 4-wire SPI while D/C# pin is not used and it must be tied to LOW. The control pins status in 3-wire SPI is shown in Table7-3.

In the write operation, a 9-bit data will be shifted into the shift register on each clock rising edge. The bit shifting sequence is D/C# bit, D7 bit, D6 bit to D0 bit. The first bit is D/C# bit which determines the following byte is command or write data. When D/C# bit is 0, the following byte is command. When D/C# bit is 1, the following byte is data. Table 7-3 shows the write procedure in 3-wire SPI

Table 7-3 : Control pins status of 3-wire SPI

Function	SCL pin	SDA pin	D/C# pin	CS# pin
Write command	↑	Command bit	Tie LOW	L
Write data	↑	Data bit	Tie LOW	L

Note:

- (1) L is connected to VSS and H is connected to VDDIO
- (2) ↑ stands for rising edge of signal



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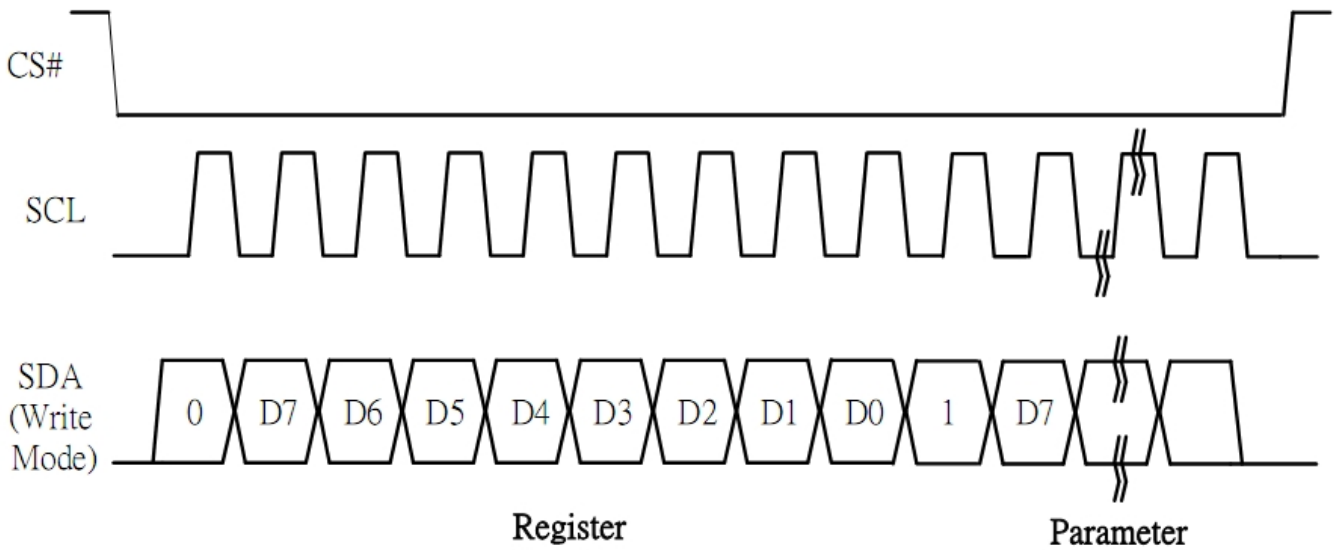


Figure 7-3 : Write procedure in 3-wire SPI

In the read operation (Register 0x1B, 0x27, 0x2D, 0x2E, 0x2F, 0x35), SDA data are transferred in the unit of 9 bits. After CS# pull low, the first byte is command byte, the D/C# bit is as 0 and following with the register byte. After command byte send, the following byte(s) are data byte(s), with D/C# bit is 1. After D/C# bit sending from MCU, an 8-bit data will be shifted out on each clock falling edge. The serial data SDA bit shifting sequence is D7, D6, to D0 bit. Figure 7-4 shows the read procedure in 3-wire SPI.

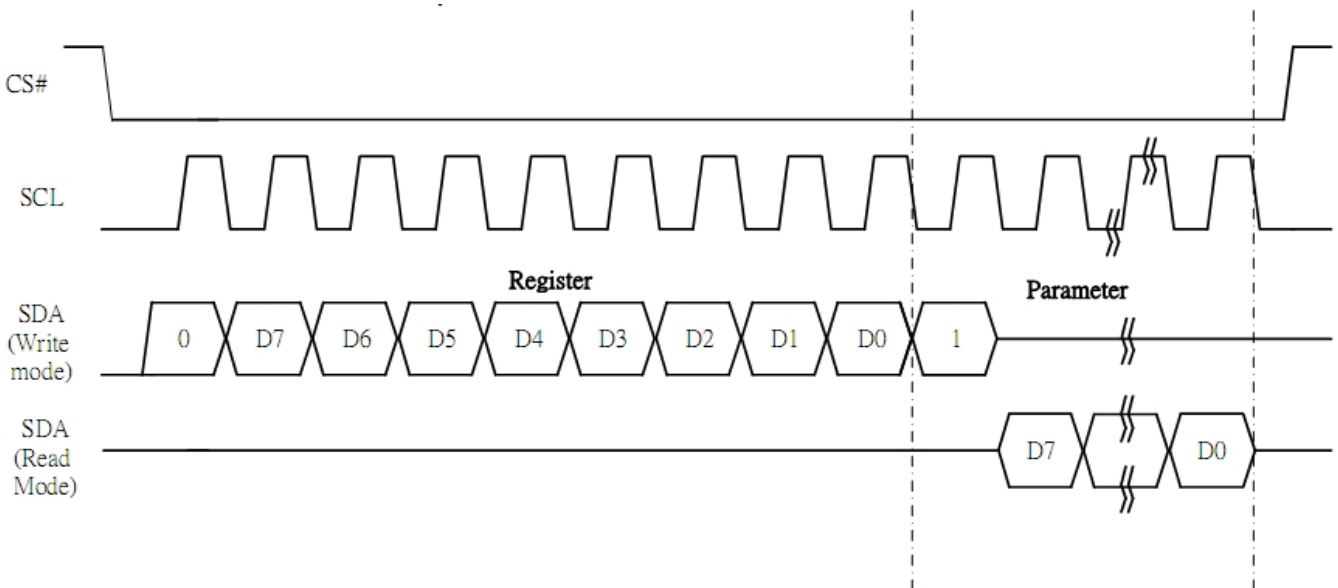


Figure 7-4 : Read procedure in 3-wire SPI mode



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8. COMMAND TABLE

Command Table											Command	Description			
R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0					
0	0	01	0	0	0	0	0	0	0	1	Driver Output control	Gate setting			
0	1		A7	A6	A5	A4	A3	A2	A1	A0		A[8:0]= 127h [POR], 296 MUX			
0	1		0	0	0	0	0	0	0	A8		MUX Gate lines setting as (A[8:0] + 1).			
0	1		0	0	0	0	0	B2	B1	B0		B[2:0] = 000 [POR].			
												Gate scanning sequence and direction			
												B[2]: GD			
												Selects the 1st output Gate			
												GD=0 [POR],			
												G0 is the 1st gate output channel, gate output sequence is G0,G1, G2, G3, ...			
												GD=1,			
												G1 is the 1st gate output channel, gate output sequence is G1, G0, G3, G2, ...			
												B[1]: SM			
												Change scanning order of gate driver.			
												SM=0 [POR],			
												G0, G1, G2, G3...295 (left and right gate interlaced)			
												SM=1,			
												G0, G2, G4 ...G294, G1, G3, ...G295			
												B[0]: TB			
												TB = 0 [POR], scan from G0 to G295			
												TB = 1, scan from G295 to G0.			
0	0	03	0	0	0	0	0	0	1	1	Gate Driving voltage Control	Set Gate driving voltage			
0	1		0	0	0	A4	A3	A2	A1	A0		A[4:0] = 00h [POR]			
												VGH setting from 10V to 20V			
												A[4:0]	VGH	A[4:0]	VGH
												00h	20	0Dh	15
												03h	10	0Eh	15.5
												04h	10.5	0Fh	16
												05h	11	10h	16.5
												06h	11.5	11h	17
												07h	12	12h	17.5
												08h	12.5	13h	18
												07h	12	14h	18.5
												08h	12.5	15h	19
												09h	13	16h	19.5
												0Ah	13.5	17h	20
												0Bh	14	Other	NA
												0Ch	14.5		



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R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	04	0	0	0	0	0	1	0	0	Source Driving voltage Control	Set Source driving voltage A[7:0] = 41h [POR], VSH1 at 15V B[7:0] = A8h [POR], VSH2 at 5V. C[7:0] = 32h [POR], VSL at -15V Remark: VSH1>=VSH2
0	1		A7	A6	A5	A4	A3	A2	A1	A0		
0	1		B7	B6	B5	B4	B3	B2	B1	B0		
0	1		C7	C6	C5	C4	C3	C2	C1	C0		

B[7] = 1,
VSH2 voltage setting from 2.4V to 8.6V

A[7]/B[7] = 0,
VSH1/VSH2 voltage setting from 8.8V to 17V

C[7] = 0,
VSL setting from -5V to -17V

A/B[7:0]	VSH1/VSH2	A/B[7:0]	VSH1/VSH2
8Eh	2.4	AFh	5.7
8Fh	2.5	B0h	5.8
90h	2.6	B1h	5.9
91h	2.7	B2h	6
92h	2.8	B3h	6.1
93h	1.54	B4h	6.2
94h	3	B5h	6.3
95h	3.1	B6h	6.4
96h	3.2	B7h	6.5
97h	3.3	B8h	6.6
98h	3.4	B9h	6.7
99h	3.5	BAh	6.8
9Ah	3.6	BBh	6.9
9Bh	3.7	BCh	7
9Ch	3.8	BDh	7.1
9Dh	3.9	BEh	7.2
9Eh	4	BFh	7.3
9Fh	4.1	C0h	7.4
A0h	4.2	C1h	7.5
A1h	4.3	C2h	7.6
A2h	4.4	C3h	7.7
A3h	4.5	C4h	7.8
A4h	4.6	C5h	7.9
A5h	4.7	C6h	8
A6h	4.8	C7h	8.1
A7h	4.9	C8h	8.2
A8h	5	C9h	8.3
A9h	5.1	CAh	8.4
AAh	5.2	CBh	8.5
ABh	5.3	CCh	8.6
ACh	5.4	CDh	8.7
ADh	5.5	CEh	8.8
A Eh	5.6	Other	NA

A/B[7:0]	VSH1/VSH2	A/B[7:0]	VSH1/VSH2
23h	9	3Ch	14
24h	9.2	3Dh	14.2
25h	9.4	3Eh	14.4
26h	9.6	3Fh	14.6
27h	9.8	40h	14.8
28h	10	41h	15
29h	10.2	42h	15.2
2Ah	10.4	43h	15.4
2Bh	10.6	44h	15.6
2Ch	10.8	45h	15.8
2Dh	11	46h	16
2Eh	11.2	47h	16.2
2Fh	11.4	48h	16.4
30h	11.6	49h	16.6
31h	11.8	4Ah	16.8
32h	12	4Bh	17
33h	12.2	Other	NA
34h	12.4		
35h	12.6		
36h	12.8		
37h	13		
38h	13.2		
39h	13.4		
3Ah	13.6		
3Bh	13.8		

C[7:0]	VSL
0Ah	-5
0Ch	-5.5
0Eh	-6
10h	-6.5
12h	-7
14h	-7.5
16h	-8
18h	-8.5
1Ah	-9
1Ch	-9.5
1Eh	-10
20h	-10.5
22h	-11
24h	-11.5
26h	-12
28h	-12.5
2Ah	-13
2Ch	-13.5
2Eh	-14
30h	-14.5
32h	-15
34h	-15.5
36h	-16
38h	-16.5
3Ah	-17
Other	NA



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R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description																												
0	0	0C	0	0	0	0	1	1	0	0	Booster Soft start	Booster Enable with Phase 1, Phase 2 and Phase 3																												
0	1		1	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀	Control	for soft start current and duration setting.																												
0	1		1	B ₆	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀		A[7:0] -> Soft start setting for Phase1 = 8Bh [POR]																												
0	1		1	C ₆	C ₅	C ₄	C ₃	C ₂	C ₁	C ₀		B[7:0] -> Soft start setting for Phase2 = 9Ch [POR]																												
0	1		0	0	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀		C[7:0] -> Soft start setting for Phase3 = 96h [POR]																												
0	1		0	0	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀		D[7:0] -> Duration setting = 0Fh [POR]																												
												Bit Description of each byte: A[6:0] / B[6:0] / C[6:0]: <table border="1" data-bbox="1018 857 1477 1196"> <thead> <tr> <th>Bit[6:4]</th> <th>Driving Strength Selection</th> </tr> </thead> <tbody> <tr><td>000</td><td>1(Weakest)</td></tr> <tr><td>001</td><td>2</td></tr> <tr><td>010</td><td>3</td></tr> <tr><td>011</td><td>4</td></tr> <tr><td>100</td><td>5</td></tr> <tr><td>101</td><td>6</td></tr> <tr><td>110</td><td>7</td></tr> <tr><td>111</td><td>8(Strongest)</td></tr> </tbody> </table>	Bit[6:4]	Driving Strength Selection	000	1(Weakest)	001	2	010	3	011	4	100	5	101	6	110	7	111	8(Strongest)										
Bit[6:4]	Driving Strength Selection																																							
000	1(Weakest)																																							
001	2																																							
010	3																																							
011	4																																							
100	5																																							
101	6																																							
110	7																																							
111	8(Strongest)																																							
												<table border="1" data-bbox="1018 1218 1477 1718"> <thead> <tr> <th>Bit[3:0]</th> <th>Min Off Time Setting of GDR [Time unit]</th> </tr> </thead> <tbody> <tr><td>0000~0011</td><td>NA</td></tr> <tr><td>0100</td><td>2.6</td></tr> <tr><td>0101</td><td>3.2</td></tr> <tr><td>0110</td><td>3.9</td></tr> <tr><td>0111</td><td>4.6</td></tr> <tr><td>1000</td><td>5.4</td></tr> <tr><td>1001</td><td>6.3</td></tr> <tr><td>1010</td><td>7.3</td></tr> <tr><td>1011</td><td>8.4</td></tr> <tr><td>1100</td><td>9.8</td></tr> <tr><td>1101</td><td>11.5</td></tr> <tr><td>1110</td><td>13.8</td></tr> <tr><td>1111</td><td>16.5</td></tr> </tbody> </table>	Bit[3:0]	Min Off Time Setting of GDR [Time unit]	0000~0011	NA	0100	2.6	0101	3.2	0110	3.9	0111	4.6	1000	5.4	1001	6.3	1010	7.3	1011	8.4	1100	9.8	1101	11.5	1110	13.8	1111	16.5
Bit[3:0]	Min Off Time Setting of GDR [Time unit]																																							
0000~0011	NA																																							
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1001	6.3																																							
1010	7.3																																							
1011	8.4																																							
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1101	11.5																																							
1110	13.8																																							
1111	16.5																																							
												D[5:0]: duration setting of phase D[5:4]: duration setting of phase 3 D[3:2]: duration setting of phase 2 D[1:0]: duration setting of phase 1 <table border="1" data-bbox="1018 1856 1477 2054"> <thead> <tr> <th>Bit[1:0]</th> <th>Duration of Phase [Approximation]</th> </tr> </thead> <tbody> <tr><td>00</td><td>10ms</td></tr> <tr><td>01</td><td>20ms</td></tr> <tr><td>10</td><td>30ms</td></tr> <tr><td>11</td><td>40ms</td></tr> </tbody> </table>	Bit[1:0]	Duration of Phase [Approximation]	00	10ms	01	20ms	10	30ms	11	40ms																		
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File Name	Specification For HINK 4.2" EPD	Module Number	HINK-E042A88
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R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description								
0	0	10	0	0	0	1	0	0	0	0	Deep Sleep mode	Deep Sleep mode Control: <table border="1"> <tr> <td>A[1:0] :</td> <td>Description</td> </tr> <tr> <td>00</td> <td>Normal Mode [POR]</td> </tr> <tr> <td>01</td> <td>Enter Deep Sleep Mode 1</td> </tr> <tr> <td>11</td> <td>Enter Deep Sleep Mode 2</td> </tr> </table> After this command initiated, the chip will enter Deep Sleep Mode, BUSY pad will keep output high. Remark: To Exit Deep Sleep mode, User required to send HWRESET to the driver	A[1:0] :	Description	00	Normal Mode [POR]	01	Enter Deep Sleep Mode 1	11	Enter Deep Sleep Mode 2
A[1:0] :	Description																			
00	Normal Mode [POR]																			
01	Enter Deep Sleep Mode 1																			
11	Enter Deep Sleep Mode 2																			
0	1		0	0	0	0	0	0	A ₁	A ₀										
0	0	11	0	0	0	1	0	0	0	1	Data Entry mode setting	Define data entry sequence A[2:0] = 011 [POR] A [1:0] = ID[1:0] Address automatic increment / decrement setting The setting of incrementing or decrementing of the address counter can be made independently in each upper and lower bit of the address. 00 -Y decrement, X decrement, 01 -Y decrement, X increment, 10 -Y increment, X decrement, 11 -Y increment, X increment [POR] A[2] = AM Set the direction in which the address counter is updated automatically after data are written to the RAM. AM= 0, the address counter is updated in the X direction. [POR] AM = 1, the address counter is updated in the Y direction.								
0	1		0	0	0	0	0	A ₂	A ₁	A ₀										
0	0	12	0	0	0	1	0	0	1	0	SW RESET	It resets the commands and parameters to their S/W Reset default values except R10h-Deep Sleep Mode During operation, BUSY pad will output high. Note: RAM are unaffected by this command.								



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R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description												
0	0	18	0	0	0	1	1	0	0	0	Temperature Sensor Control	Temperature Sensor Selection A[7:0] = 48h [POR], external temperature sensor A[7:0] = 80h Internal temperature sensor												
0	1		A7	A6	A5	A4	A3	A2	A1	A0														
0	0	1A	0	0	0	1	1	0	1	0	Temperature Sensor Control (Write to temperature register)	Write to temperature register. A[11:0] = 7FFh [POR]												
0	1		A7	A6	A5	A4	A3	A2	A1	A0														
0	0	1B	0	0	0	1	1	0	1	1	Temperature Sensor Control (Read from temperature register)	Read from temperature register.												
1	1		A7	A6	A5	A4	A3	A2	A1	A0														
0	0	20	0	0	1	0	0	0	0	0	Master Activation	Activate Display Update Sequence The Display Update Sequence Option is located at R22h. BUSY pad will output high during operation. User should not interrupt this operation to avoid corruption of panel images.												
0	0	21	0	0	1	0	0	0	0	1	Display Update Control ¹	RAM content option for Display Update A[7:0] = 00h [POR] B[7:0] = 00h [POR] A[7:4] Red RAM option <table border="1"> <tr><td>0000</td><td>Normal</td></tr> <tr><td>0100</td><td>Bypass RAM content as 0</td></tr> <tr><td>1000</td><td>Inverse RAM content</td></tr> </table> A[3:0] Red RAM option <table border="1"> <tr><td>0000</td><td>Normal</td></tr> <tr><td>0100</td><td>Bypass RAM content as 0</td></tr> <tr><td>1000</td><td>Inverse RAM content</td></tr> </table>	0000	Normal	0100	Bypass RAM content as 0	1000	Inverse RAM content	0000	Normal	0100	Bypass RAM content as 0	1000	Inverse RAM content
0000	Normal																							
0100	Bypass RAM content as 0																							
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0100	Bypass RAM content as 0																							
1000	Inverse RAM content																							
0	1		A7	A6	A5	A4	A3	A2	A1	A0														
0	1		B7	0	0	0	0	0	0	0														



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R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description																										
0	0	22	0	0	1	0	0	0	1	0	Display Update Control 2	Display Update Sequence Option: Enable the stage for Master Activation A[7:0]= FFh (POR)																										
			A7	A6	A5	A4	A3	A2	A1	A0		<table border="1"> <thead> <tr> <th>Operating sequence</th> <th>Parameter (in Hex)</th> </tr> </thead> <tbody> <tr> <td>Enable clock signal</td> <td>80</td> </tr> <tr> <td>Disable clock signal</td> <td>01</td> </tr> <tr> <td>Enable clock signal Enable Analog</td> <td>C0</td> </tr> <tr> <td>Disable Analog Disable clock signal</td> <td>03</td> </tr> <tr> <td>Enable clock signal Load LUT with DISPLAY Mode 1 Disable clock signal</td> <td>91</td> </tr> <tr> <td>Enable clock signal Load LUT with DISPLAY Mode 2 Disable clock signal</td> <td>99</td> </tr> <tr> <td>Enable clock signal Load temperature value Load LUT with DISPLAY Mode 1 Disable clock signal</td> <td>B1</td> </tr> <tr> <td>Enable clock signal Load temperature value Load LUT with DISPLAY Mode 2 Disable clock signal</td> <td>B9</td> </tr> <tr> <td>Enable clock signal Enable Analog Display with DISPLAY Mode 1 Disable Analog Disable OSC</td> <td>C7</td> </tr> <tr> <td>Enable clock signal Enable Analog Display with DISPLAY Mode 2 Disable Analog Disable OSC</td> <td>CF</td> </tr> <tr> <td>Enable clock signal Enable Analog Load temperature value DISPLAY with DISPLAY Mode 1 Disable Analog Disable OSC</td> <td>F7</td> </tr> <tr> <td>Enable clock signal Enable Analog Load temperature value DISPLAY with DISPLAY Mode 2 Disable Analog Disable OSC</td> <td>FF</td> </tr> </tbody> </table>	Operating sequence	Parameter (in Hex)	Enable clock signal	80	Disable clock signal	01	Enable clock signal Enable Analog	C0	Disable Analog Disable clock signal	03	Enable clock signal Load LUT with DISPLAY Mode 1 Disable clock signal	91	Enable clock signal Load LUT with DISPLAY Mode 2 Disable clock signal	99	Enable clock signal Load temperature value Load LUT with DISPLAY Mode 1 Disable clock signal	B1	Enable clock signal Load temperature value Load LUT with DISPLAY Mode 2 Disable clock signal	B9	Enable clock signal Enable Analog Display with DISPLAY Mode 1 Disable Analog Disable OSC	C7	Enable clock signal Enable Analog Display with DISPLAY Mode 2 Disable Analog Disable OSC	CF	Enable clock signal Enable Analog Load temperature value DISPLAY with DISPLAY Mode 1 Disable Analog Disable OSC	F7	Enable clock signal Enable Analog Load temperature value DISPLAY with DISPLAY Mode 2 Disable Analog Disable OSC	FF
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Enable clock signal Enable Analog Load temperature value DISPLAY with DISPLAY Mode 2 Disable Analog Disable OSC	FF																																					
0	0	24	0	0	1	0	0	1	0	0	Write RAM (Black White) / RAM 0x24	<p>After this command, data entries will be written into the BW RAM until another command is written. Address pointers will advance accordingly</p> <p>For Write pixel: Content of Write RAM(BW) = 1 For Black pixel: Content of Write RAM(BW) = 0</p>																										



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R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description																																																																
0	0	26	0	0	1	0	0	1	1	0	Write RAM (RED) / RAM 0x26	<p>After this command, data entries will be written into the RED RAM until another command is written. Address pointers will advance accordingly.</p> <p>For Red pixel: Content of Write RAM(RED) = 1 For non-Red pixel [Black or White]: Content of Write RAM(RED) = 0</p>																																																																
0	0	27	0	0	1	0	0	1	1	1	Read RAM	<p>After this command, data read on the MCU bus will fetch data from RAM. According to parameter of Register 41h to select reading RAM0x24/ RAM0x26, until another command is written. Address pointers will advance accordingly.</p> <p>The 1st byte of data read is dummy data.</p>																																																																
0	0	2C	0	0	1	0	1	1	01	0	Write VCOM register	<p>Write VCOM register from MCU interface A[7:0] = 00h [POR].</p> <table border="1"> <thead> <tr> <th>A[7:0]</th> <th>VCOM</th> <th>A[7:0]</th> <th>VCOM</th> </tr> </thead> <tbody> <tr><td>08h</td><td>-0.2</td><td>44h</td><td>-1.7</td></tr> <tr><td>0Ch</td><td>-0.3</td><td>48h</td><td>-1.8</td></tr> <tr><td>10h</td><td>-0.4</td><td>4Ch</td><td>-1.9</td></tr> <tr><td>14h</td><td>-0.5</td><td>50h</td><td>-2</td></tr> <tr><td>18h</td><td>-0.6</td><td>54h</td><td>-2.1</td></tr> <tr><td>1Ch</td><td>-0.7</td><td>58h</td><td>-2.2</td></tr> <tr><td>20h</td><td>-0.8</td><td>5Ch</td><td>-2.3</td></tr> <tr><td>24h</td><td>-0.9</td><td>60h</td><td>-2.4</td></tr> <tr><td>28h</td><td>-1</td><td>64h</td><td>-2.5</td></tr> <tr><td>2Ch</td><td>-1.1</td><td>68h</td><td>-2.6</td></tr> <tr><td>30h</td><td>-1.2</td><td>6Ch</td><td>-2.7</td></tr> <tr><td>34h</td><td>-1.3</td><td>70h</td><td>-2.8</td></tr> <tr><td>38h</td><td>-1.4</td><td>74h</td><td>-2.9</td></tr> <tr><td>3Ch</td><td>-1.5</td><td>78h</td><td>-3</td></tr> <tr><td>40h</td><td>-1.6</td><td>Other</td><td>NA</td></tr> </tbody> </table>	A[7:0]	VCOM	A[7:0]	VCOM	08h	-0.2	44h	-1.7	0Ch	-0.3	48h	-1.8	10h	-0.4	4Ch	-1.9	14h	-0.5	50h	-2	18h	-0.6	54h	-2.1	1Ch	-0.7	58h	-2.2	20h	-0.8	5Ch	-2.3	24h	-0.9	60h	-2.4	28h	-1	64h	-2.5	2Ch	-1.1	68h	-2.6	30h	-1.2	6Ch	-2.7	34h	-1.3	70h	-2.8	38h	-1.4	74h	-2.9	3Ch	-1.5	78h	-3	40h	-1.6	Other	NA
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0	1		A7	A6	A5	A4	A3	A2	A1	A0																																																																		



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R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description	
0	0	3C	0	0	1	1	1	1	0	0	Border Waveform Control	Select border waveform for VBD A[7:0] = C0h [POR], set VBD as HiZ. A [7:6] :Select VBD option	
0	1		A ₇	A ₆	A ₅	A ₄	0	A ₂	A ₁	A ₀		A[7:6]	Select VBD as
												00	GS Transition, Defined in A[2] and A[1:0]
												01	Fix Level, Defined in A[5:4]
												10	VCOM
												11[POR]	HiZ
												A [5:4] Fix Level Setting for VBD	
												A[5:4]	VBD level
												00	VSS
												01	VSH1
												10	VSL
												11	VSH2
												A [1:0] GS Transition setting for VBD VBD Level Selection: 00b: VCOM ; 01b: VSH1; 10b: VSL; 11b: VSH2	
												A[1:0]	VBD Transition
												00	LUT0
											01	LUT1	
											10	LUT2	
											11	LUT3	
0	0	41	0	1	0	0	0	0	0	1	Read RAM Option	Read RAM Option A[0]= 0 [POR] 0: Read RAM corresponding to RAM0x24 1: Read RAM corresponding to RAM0x26	
0	1		0	0	0	0	0	0	0	A ₀			
0	0	44	0	1	0	0	0	1	0	0	Set RAM X - address Start / End position	Specify the start/end positions of the window address in the X direction by an address unit for RAM A[5:0]: XSA[5:0], XStart, POR = 00h B[5:0]: XEA[5:0], XEnd, POR = 31h	
0	1		0	0	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀			
0	1		0	0	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀			
0	0	45	0	1	0	0	0	1	0	1	Set Ram Y- address Start / End position	Specify the start/end positions of the window address in the Y direction by an address unit for RAM A[8:0]: YSA[8:0], YStart, POR = 000h B[8:0]: YEA[8:0], YEnd, POR = 12Bh	
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀			
0	1		0	0	0	0	0	0	0	A ₈			
0	1		B ₇	B ₆	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀			
0	1		0	0	0	0	0	0	0	B ₈			



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R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description																																											
0	0	46	0	1	0	0	0	1	1	0	Auto Write RED RAM for Regular Pattern	Auto Write RED RAM for Regular Pattern A[7:0] = 00h [POR]																																											
0	1		A7	A6	A5	A4	0	A2	A1	A0	Regular Pattern	A[7]: The 1st step value, POR = 0 A[6:4]: Step Height, POR= 000 Step of alter RAM in Y-direction according to Gate <table border="1"> <thead> <tr> <th>A[6:4]</th> <th>Height</th> <th>A[6:4]</th> <th>Height</th> </tr> </thead> <tbody> <tr> <td>000</td> <td>8</td> <td>100</td> <td>128</td> </tr> <tr> <td>001</td> <td>16</td> <td>101</td> <td>256</td> </tr> <tr> <td>010</td> <td>32</td> <td>110</td> <td>300</td> </tr> <tr> <td>011</td> <td>64</td> <td>111</td> <td>NA</td> </tr> </tbody> </table> A[2:0]: Step Width, POR= 000 Step of alter RAM in X-direction according to Source <table border="1"> <thead> <tr> <th>A[2:0]</th> <th>Width</th> <th>A[2:0]</th> <th>Width</th> </tr> </thead> <tbody> <tr> <td>000</td> <td>8</td> <td>100</td> <td>128</td> </tr> <tr> <td>001</td> <td>16</td> <td>101</td> <td>256</td> </tr> <tr> <td>010</td> <td>32</td> <td>110</td> <td>400</td> </tr> <tr> <td>011</td> <td>64</td> <td>111</td> <td>NA</td> </tr> </tbody> </table> BUSY pad will output high during operation.				A[6:4]	Height	A[6:4]	Height	000	8	100	128	001	16	101	256	010	32	110	300	011	64	111	NA	A[2:0]	Width	A[2:0]	Width	000	8	100	128	001	16	101	256	010	32	110	400	011	64	111	NA
A[6:4]	Height	A[6:4]	Height																																																				
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0	0	47	0	1	0	0	0	1	1	1	Auto Write B/W RAM for Regular Pattern	Auto Write B/W RAM for Regular Pattern A[7:0] = 00h [POR]																																											
0	1		A7	A6	A5	A4	0	A2	A1	A0	Regular Pattern	A[7]: The 1st step value, POR = 0 A[6:4]: Step Height, POR= 000 Step of alter RAM in Y-direction according to Gate <table border="1"> <thead> <tr> <th>A[6:4]</th> <th>Height</th> <th>A[6:4]</th> <th>Height</th> </tr> </thead> <tbody> <tr> <td>000</td> <td>8</td> <td>100</td> <td>128</td> </tr> <tr> <td>001</td> <td>16</td> <td>101</td> <td>256</td> </tr> <tr> <td>010</td> <td>32</td> <td>110</td> <td>300</td> </tr> <tr> <td>011</td> <td>64</td> <td>111</td> <td>NA</td> </tr> </tbody> </table> A[2:0]: Step Width, POR= 000 Step of alter RAM in X-direction according to Source <table border="1"> <thead> <tr> <th>A[2:0]</th> <th>Width</th> <th>A[2:0]</th> <th>Width</th> </tr> </thead> <tbody> <tr> <td>000</td> <td>8</td> <td>100</td> <td>128</td> </tr> <tr> <td>001</td> <td>16</td> <td>101</td> <td>256</td> </tr> <tr> <td>010</td> <td>32</td> <td>110</td> <td>400</td> </tr> <tr> <td>011</td> <td>64</td> <td>111</td> <td>NA</td> </tr> </tbody> </table> During operation, BUSY pad will output high.				A[6:4]	Height	A[6:4]	Height	000	8	100	128	001	16	101	256	010	32	110	300	011	64	111	NA	A[2:0]	Width	A[2:0]	Width	000	8	100	128	001	16	101	256	010	32	110	400	011	64	111	NA
A[6:4]	Height	A[6:4]	Height																																																				
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R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	4E	0	1	0	0	1	1	1	0	Set RAM X address counter	Make initial settings for the RAM X address in the address counter (AC) A[5:0]: 00h [POR].
0	1		0	0	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		
0	0	4F	0	1	0	0	1	1	1	1	Set RAM Y address counter	Make initial settings for the RAM Y address in the address counter (AC) A[8:0]: 000h [POR].
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		
0	1		0	0	0	0	0	0	0	A ₈		



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9. DATA ENTRY MODE SETTING (11H)

This command has multiple configurations and each bit setting is described as follows:

R/W	DC	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1						AM	ID1	IDO
POR		0	0	0	0	0	0	1	1

ID[1:0]: The address counter is automatically incremented by 1, after data is written to the RAM when ID[1:0] = "01". The address counter is automatically decremented by 1, after data is written to the RAM when ID[1:0] = "00". The setting of incrementing or decrementing of the address counter can be made independently in each upper and lower bit of the address. The direction of the address when data is written to the RAM is set by AM bits.

AM: Set the direction in which the address counter is updated automatically after data are written to the RAM. When AM = "0", the address counter is updated in the X direction. When AM = "1", the address counter is updated in the Y direction. When window addresses are selected, data are written to the RAM area specified by the window addresses in the manner specified with ID[1:0] and AM bits.

	ID [1:0]="00" X: decrement Y: decrement	ID [1:0]="01" X: increment Y: decrement	ID [1:0]="10" X: decrement Y: increment	ID [1:0]="11" X: increment Y: increment
AM="0" X-mode				
AM="1" Y-mode				

The pixel sequence is defined by the ID [0].

	ID [1:0]="00" X: decrement Y: decrement	ID [1:0]="01" X: increment Y: decrement
AM="0" X-mode		



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10. REFERENCE CIRCUIT

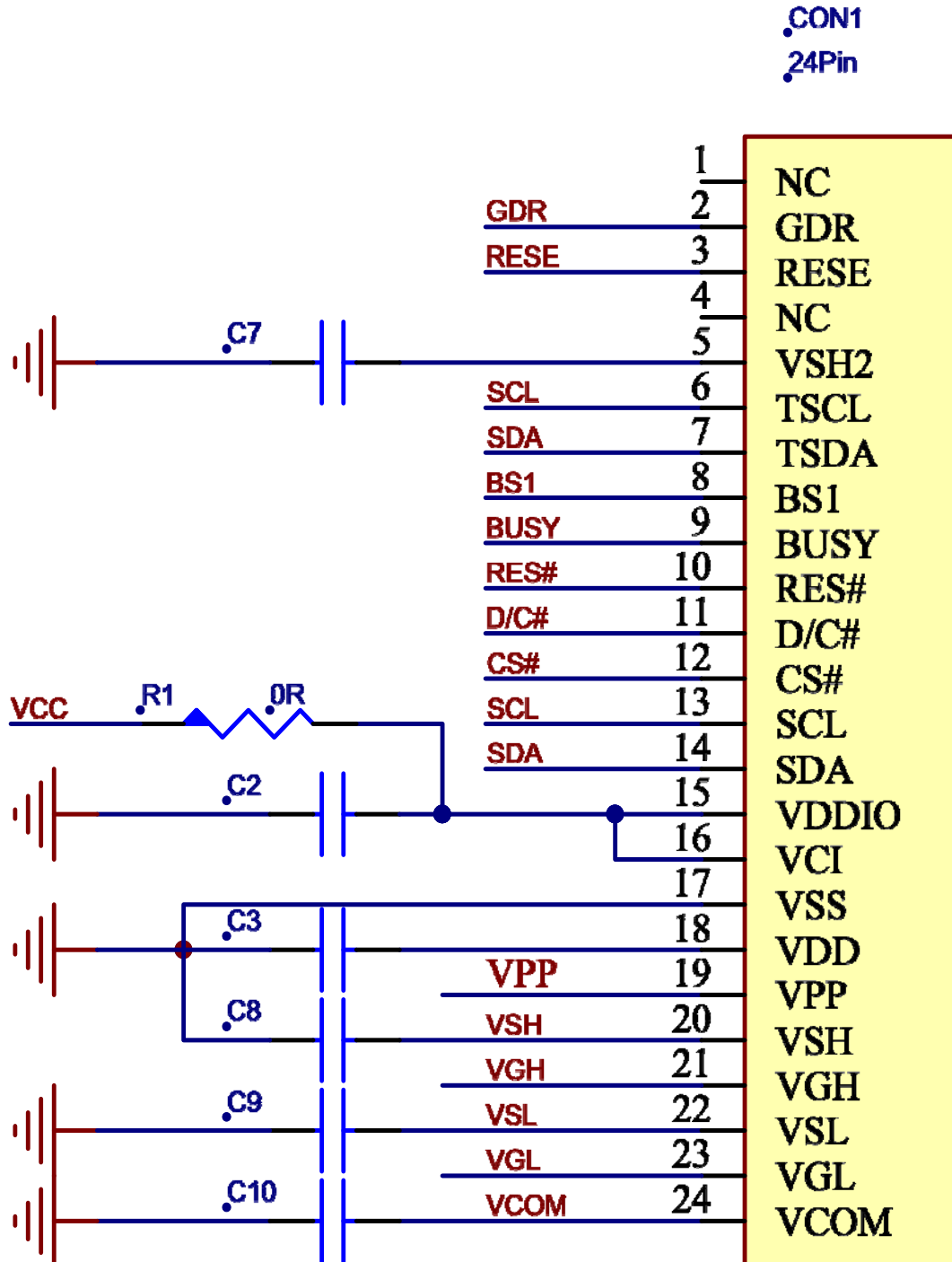


Figure. 10-1



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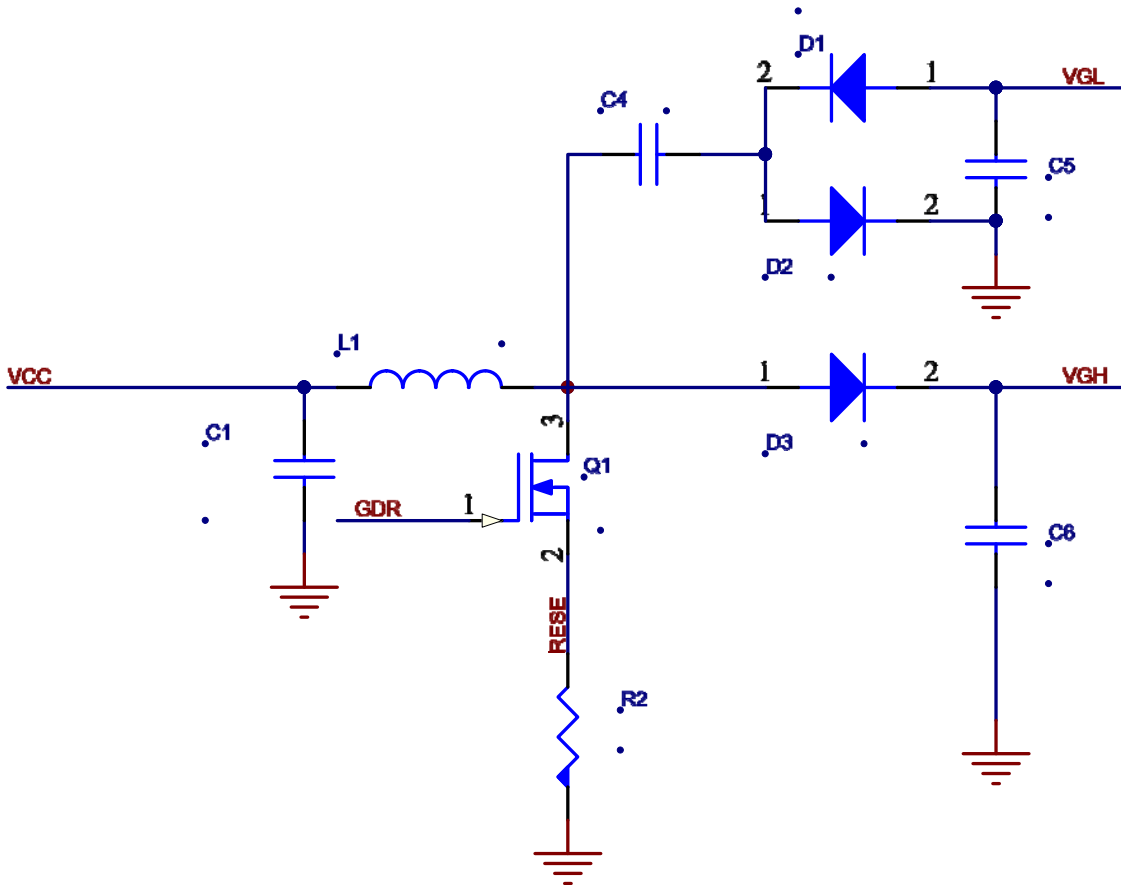


Figure. 10-2

Part Name	Value /requirement/Reference Part
C1—C10	1uF/0603;X5R/X7R;Voltage Rating: 25V
C10	1uF/0603;X7R;Voltage Rating: 25V
D1—D3	MBR0530 1) Reverse DC voltage $\geq 30V$ 2) Forward current $\geq 500mA$ 3) Forward voltage $\leq 430mV$
R2	2.2 Ω /0603: 1% variation
Q1	NMOS:Si1304BDL/NX3008NBK 1) Drain-Source breakdown voltage $\geq 30V$ 2) $V_{gs} (th) = 0.9 (Typ) , 1.3V (Max)$ 3) $R_{ds on} \leq 2.1 \Omega @ V_{gs}=2.5V$
L1	47uH/CDRH2D18、LDNP-470NC Maximum DC current~420mA Maximum DC resistance~650m Ω
CON24Pin	24Pins,0.5mm pitch ZIF Socket



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11. ABSOLUTE MAXIMUM RATING

Table 10-1 : Maximum Ratings

Symbol	Parameter	Rating	Unit	Humidity	Unit	Note
V _{CI}	Logic supply voltage	-0.5 to +6.0	V	-	-	
T _{OPR}	Operation temperature range	0 to 40	°C	45 to70	%	Note 11-1
T _{tgt}	Transportation temperature range	-25 to 60	°C	45 to70	%	Note11-2
T _{stg}	Storage condition	0 to 40	°C	45 to70	%	Maximum storage time: 5 years
-	After opening the package	0 to 40	°C	45 to70	%	

Note 11-1: We guarantee the single pixel display quality for 0-35°C, but we only guarantee the barcode readable for 35-40°C.

Normal use is recommended to refresh every 24 hours.

Note11-2: T_{tgt} is the transportation condition, the transport time is within 10 days for -25°C~0°C or 40°C~60°C.

Note 11-3: When the three-color product is stored. The display screen should be kept white and face up. In addition, please be sure to refresh the e-paper every three months. We suggest that the full black and full white picture could be added to clear the screen after the module is refreshed for a long time, the display effect would be better.

12. DC CHARACTERISTICS

The following specifications apply for: VSS=0V, VCI=3.0V, T_{OPR}=25°C.

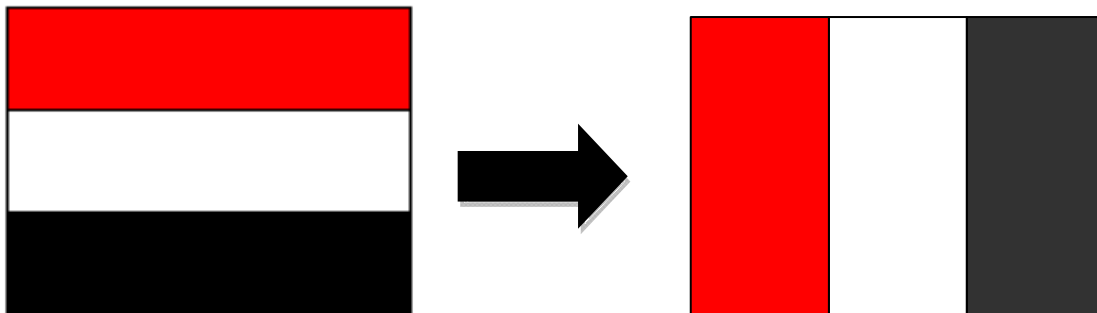
Table 11-1: DC Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V _{CI}	VCI operation voltage	-	2.5	3.0	3.7	V
V _{IH}	High level input voltage	-	0.8VDDIO	-	-	V
V _{IL}	Low level input voltage	-	-	-	0.2VDDIO	V
V _{OH}	High level output voltage	I _{OH} = -100uA	0.9VDDIO	-	-	V
V _{OL}	Low level output voltage	I _{OL} = 100uA	-	-	0.1VDDIO	V
I _{update}	Module operating current	-	-	6	-	mA
I _{sleep}	Deep sleep mode	VCI=3.3V	-	-	3	uA

- The Typical power consumption is measured using associated 25°C waveform with following pattern transition: from horizontal scan pattern to vertical scan pattern. (Note 12-1)
- The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by XingTai.
- Vcom value will be OTP before in factory or present on the label sticker.

Note 12-1

The Typical power consumption





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13. AC CHARACTERISTICS

The following specifications apply for: VDDIO - VSS = 2.5V to 3.7V, TOPR = 25°C

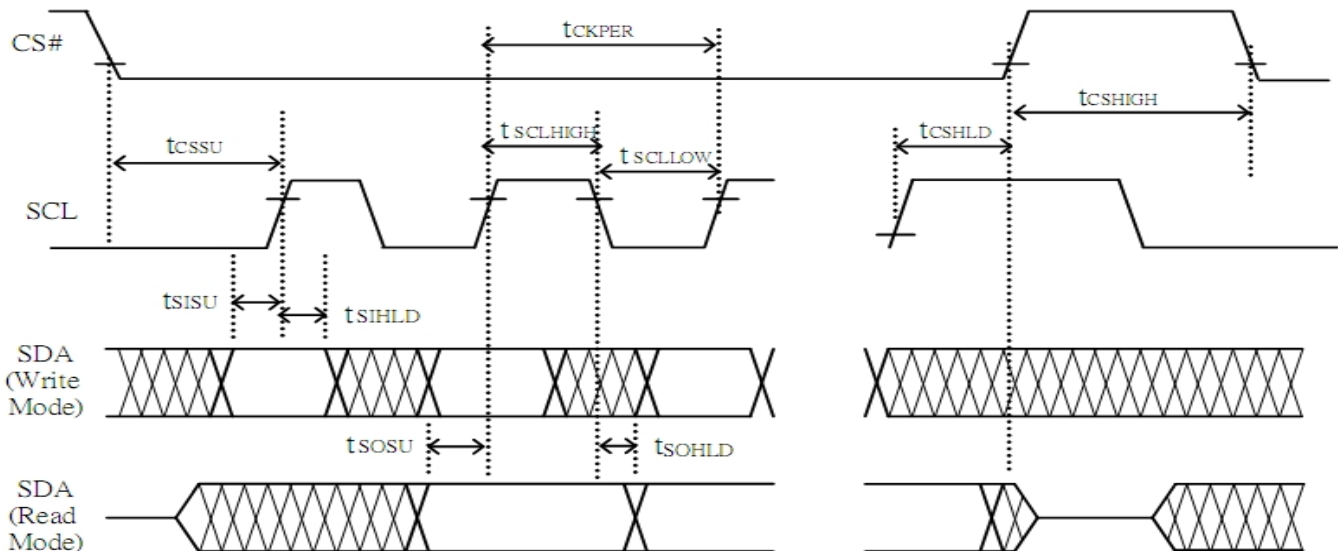
Write mode

Symbol	Parameter	Min	Typ	Max	Unit
fSCL	SCL frequency (Write Mode)	-	-	20	MHz
tCSSU	Time CS# has to be low before the first rising edge of SCLK	TBD	-	-	ns
tCSHLD	Time CS# has to remain low after the last falling edge of SCLK	TBD	-	-	ns
tCSHIGH	Time CS# has to remain high between two transfers	TBD	-	-	ns
tSCLHIGH	Part of the clock period where SCL has to remain high	TBD	-	-	ns
tSCLLOW	Part of the clock period where SCL has to remain low	TBD	-	-	ns
tSISU	Time SI (SDA Write Mode) has to be stable before the next rising edge of SCL	TBD	-	-	ns
tSIHLD	Time SI (SDA Write Mode) has to remain stable after the rising edge of SCL	TBD	-	-	ns

Read mode

Symbol	Parameter	Min	Typ	Max	Unit
fSCL	SCL frequency (Read Mode)	-	-	2.5	MHz
tCSSU	Time CS# has to be low before the first rising edge of SCLK	TBD	-	-	ns
tCSHLD	Time CS# has to remain low after the last falling edge of SCLK	TBD	-	-	ns
tCSHIGH	Time CS# has to remain high between two transfers	TBD	-	-	ns
tSCLHIGH	Part of the clock period where SCL has to remain high	TBD	-	-	ns
tSCLLOW	Part of the clock period where SCL has to remain low	TBD	-	-	ns
tSOSU	Time SO(SDA Read Mode) will be stable before the next rising edge of SCL	-	TBD	-	ns
tSOHLD	Time SO (SDA Read Mode) will remain stable after the falling edge of SCL	-	TBD	-	ns

Note: All timings are based on 20% to 80% of VDDIO-VSS



14. POWER CONSUMPTION

Parameter	Symbol	Conditions	TYP	Max	Unit	Remark
Panel power consumption during update	-	25°C	-	240	mAs	-
Deep sleep mode	-	25°C	-	3	uA	-

MAs=update average current ×update time



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15. TYPICAL OPERATING SEQUENCE

POWER ON			
Step	Action	Value/Data	Comment
1	VCI	3V	Power on
2	Delay	10ms	Wait for power on

Init Config			
Step	Action	Value/Data	Comment
1	BS1	Output: LOW	Initial pin config For 4-wire SPI,BS1=0 and D/C pin is controlled by MCU for Data/Cmmand For 3-wire SPI,BS1=1 and D/C pin is fix to 0
2	CS#	Output: HIGH	
3	D/C#	Output: LOW	
4	SCL	Output: LOW	
5	SDA	Input	
6	BUSY	Input	
7	RES#	HIGH	HWRESET: Hardware Reset
8	RES#	LOW	
9	Delay	200us	
10	RES#	HIGH	
11	Wait for BUSY Low	Bound by a timeout value	
12	Command 0x12	-	SWRESET: Software Reset
13	Wait for BUSY Low	Bound by a timeout value	Max. wait 10ms

Init Code			
Step	Action	Value/Data	Comment
1	Command 0x01	0x2B,0x01,0x00	Set Driver Output Control for Gate setting = Gate Channel - 1 For example, for 300 gate channel => 300 - 1 = 299 (0x12B)
2	Command 0x11	0x01	Set Data Entry Mode setting, Y decrement, X increment, address counter in X-direction
3	Command 0x44	0x00, 0x31	Set RAM X address, start position = 0 and end position = Source Channel/8 - 1 => 49(0x31)
4	Command 0x45	0x2B,0x01,0x00,0x00	Set RAM Y address, start position = 300 - 1 = 299 (0x12B) and end position = 05Command
5	Command 0x3C	Black: 0x00 White: 0x01 VCOM: 0x80 Hiz: 0xC0(Default)	Set Border [0x80 keep as previous]



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Write BW image data in Reg 0x24 and Red image data in Reg 0x26, Set softstart control

Step	Action	Value/Data	Comment
1	Command 0x4E	0x00	Set RAM X address counter = 02Command
2	Command 0x4F	0x2B,0x01	Set Driver Output Control for Gate setting = Gate Channel - 1 For example, for 300 gate channel => 300 - 1 = 299 (0x12B)
3	Command 0x24	0xXX,..., 0xXX	Write B/W image data into to Register 0x24 RAM Total number of Bytes = (Source Channel x Gate Channel) / 8
4	Command 0x4E	0x00	Set RAM X address counter = 02Command
5	Command 0x4F	0x2B,0x01	Set Driver Output Control for Gate setting = Gate Channel - 1 For example, for 300 gate channel => 300 - 1 = 299 (0x12B)
6	Command 0x26	0xXX,..., 0xXX	Write Red image data into Register 0x26 RAM Total number of Bytes = (Source Channel x Gate Channel) / 8
7	Command 0x0C	0xXX , 0xXX, 0xXX, 0xXX	Set softstart setting(Remark: it is optional. If the default setting is fin, user is no need to set it)

Sense temperature by internal temperature sensor, load waveform LUT from OTP and Drive display panel

Step	Action	Value/Data	Comment
8	Command 0x18	0x80	Select internal temperature sensor
9	Command 0x22	0Xf7	Set Display update control: Enable clock, load TS value, load LUT from OTP==> Enable analog ==>Display panel according to display mode selection set by bit[A3] ==> Off analog ==> Off clock; Bit[A3] = 0to select LUT.
10	Command 0x20		Master Activation: Run display update sequence which is defined by Command 0x22
11	Wait for BUSY Low	Bound by a timeout value	

Deep Sleep and Power off

Step	Action	Value/Data	Comment
1	Command 0x10	0x01	Deep sleep



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16. OPTICAL CHARACTERISTICS

16.1 Specifications

Measurements are made with that the illumination is under an angle of 45 degrees, the detection is perpendicular unless otherwise specified.

T=25°C

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT	Note
R	Reflectance	White	30	35	-	%	Note 16-1
Gn	2Grey Level	-	-	$KS+(WS-KS) \times n(m-1)$	-	L*	-
CR	Contrast Ratio	-	10	15	-		-
KS	Black State L* value		-	13	14		Note 16-1
	Black State a* value		-	3	4		Note 16-1
WS	White State L* value		63	65	-		Note 16-1
RS	Red State L* value	Red	25	28	-		Note 16-1
	Red State a* value	Red	36	40	-		Note 16-1
Panel	Image Update	Storage and transportation	-	Update the white screen	-	-	-
	Update Time	Operation	-	Suggest Updated once a day	-	-	-

WS : White state, KS : Black state, RS: Red state

Note 16-1 : Luminance meter : i - One Pro Spectrophotometer

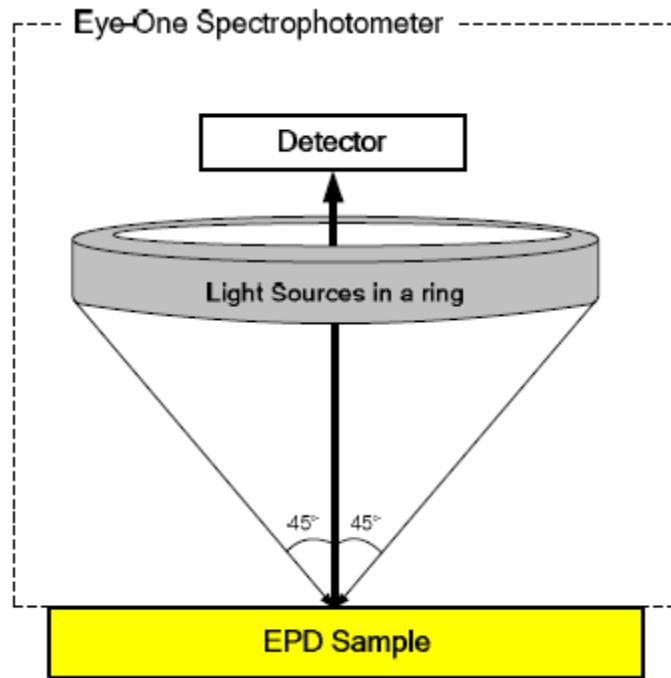


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16.2 Definition of contrast ratio

The contrast ratio (CR) is the ratio between the reflectance in a full white area (Rl) and the reflectance in a dark area (Rd):

$$CR = Rl/Rd$$

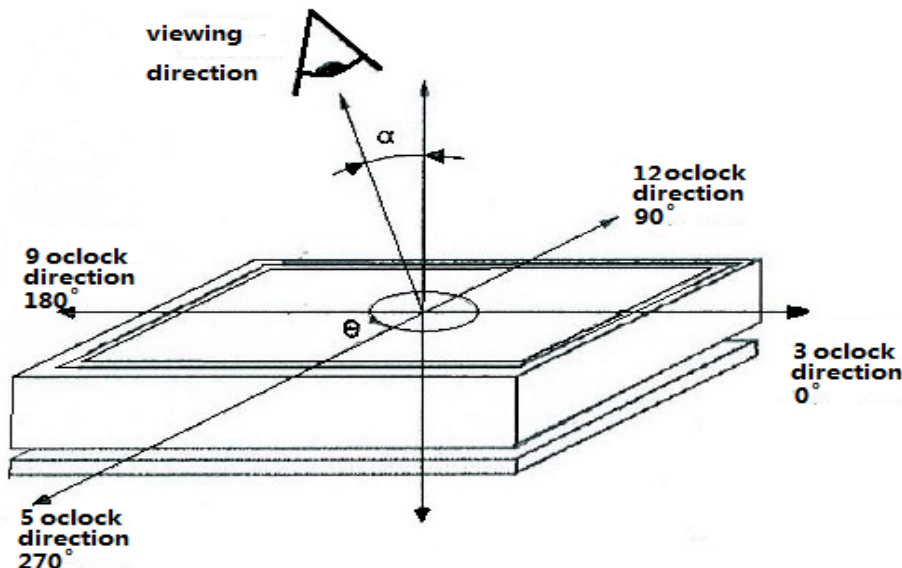


16.3 Reflection Ratio

The reflection ratio is expressed as:

$$R = \text{Reflectance Factor}_{\text{white board}} \times (L_{\text{center}} / L_{\text{white board}})$$

L_{center} is the luminance measured at center in a white area ($R=G=B=1$). $L_{\text{white board}}$ is the luminance of a standard white board. Both are measured with equivalent illumination source. The viewing angle shall be no more than 2 degrees.





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17. HANDLING, SAFETY AND ENVIROMENTAL REQUIREMENTS

WARNING

The display module should be kept flat or fixed to a rigid, curved support with limited bending along the long axis. It should not be used for continual flexing and bending. Handle with care. Should the display break do not touch any material that leaks out. In case of contact with the leaked material then wash with water and soap.

CAUTION

The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.

Disassembling the display module can cause permanent damage and invalidate the warranty agreements.

IPA solvent can only be applied on active area and the back of a glass. For the rest part, it is not allowed.

Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged . Moreover the display is sensitive to static electricity and other rough environmental conditions.

Mounting Precautions

(1) It's recommended that you consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the module.

(2) It's recommended that you attach a transparent protective plate to the surface in order to protect the EPD. Transparent protective plate should have sufficient strength in order to resist external force.

(3) You should adopt radiation structure to satisfy the temperature specification.

(4) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the PS at high temperature and the latter causes circuit break by electro-chemical reaction.

(5) Do not touch, push or rub the exposed PS with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment. Do not touch the surface of PS for bare hand or greasy cloth. (Some cosmetics deteriorate the PS)

(6) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach the PS. Do not use acetone, toluene and alcohol because they cause chemical damage to the PS.

(7) Wipe off saliva or water drops as soon as possible. Their long time contact with PS causes deformations and color fading.

Data sheet status

Product specification	The data sheet contains final product specifications.
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Limiting values

Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information

Where application information is given, it is advisory and does not form part of the specification.

Product Environmental certification

ROHS

REMARK

All The specifications listed in this document are guaranteed for module only. Post-assembled operation or component(s) may impact module performance or cause unexpected effect or damage and therefore listed specifications is not warranted after any Post-assembled operation.



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18. RELIABILITY TEST

18.1 Reliability Test Items

	TEST	CONDITION	REMARK
1	High-Temperature Operation	T=40°C, RH=35%RH, For 240Hr	
2	Low-Temperature Operation	T = 0°C for 240 hrs	
3	High-Temperature Storage	T=50°C RH=35%RH For 240Hr	Test in white pattern
4	Low-Temperature Storage	T = -25°C for 240 hrs	Test in white pattern
5	High Temperature, High-Humidity Operation	T=40°C, RH=90%RH, For 168Hr	
6	High Temperature, High-Humidity Storage	T=50°C, RH=80%RH, For 240Hr Test in white pattern	Test in white pattern
7	Temperature Cycle	-25°C(30min)~60°C(30min), 50 Cycle	Test in white pattern
8	Package Vibration	1.04G, Frequency : 20~200Hz Direction : X,Y,Z Duration: 30 minutes in each direction	Full packed for shipment
9	Package Drop Impact	Drop from height of 100 cm on Concrete surface Drop sequence: 1 corner, 3 edges, 6 face One drop for each.	Full packed for shipment
10	UV exposure Resistance	765 W/m ² for 168hrs, 40°C	
11	Electrostatic discharge	Machine model: +/-250V, 0Ω, 200pF	

Actual EMC level to be measured on customer application.

Note1: Stay white pattern for storage and non-operation test.

Note2: Operation is black/white/red pattern, hold time is 150S.

Note3: The function, appearance, opticals should meet the requirements of the test before and after the test.

Note4: Keep testing after 2 hours placing at 20°C-25°C.

18.2 Product life time

The EPD Module is designed for a 5-year life-time with 25 °C/60%RH operation assumption. Reliability estimation testing with accelerated life-time theory would be demonstrated to provide confidence of EPD lifetime.

18.3 Product warranty

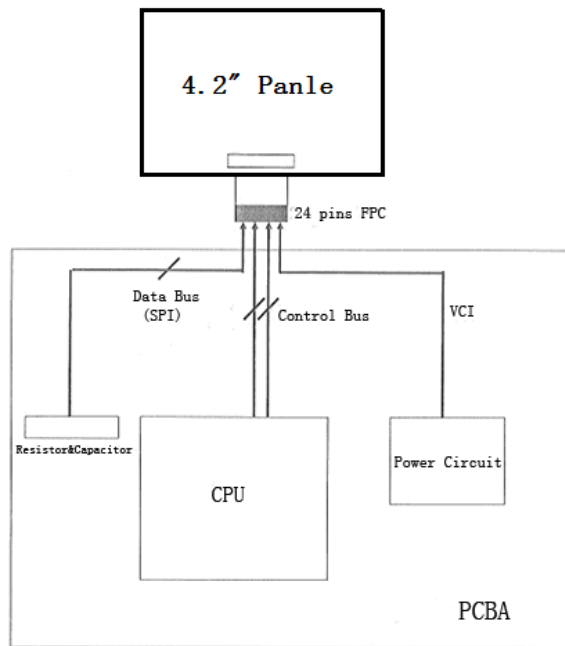
Warranty conditions have to be negotiated between Xingtai and individual customers.

Xingtai provides 12+1(one month delivery time) months warranty for all products which are purchased from Xingtai.

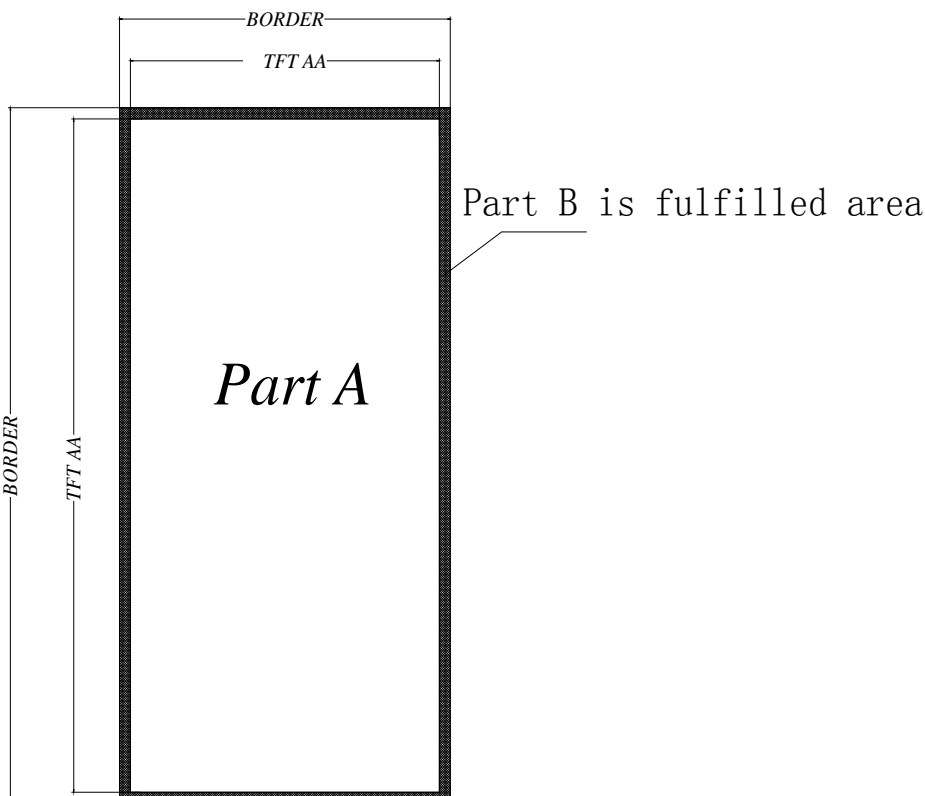


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19. BLOCK DIAGRAM



20. PARTA/PARTB SPECIFICATION





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21. POINT AND LINE STANDARD

Shipment Inspection Standard						
Equipment: Electrical test fixture, Point gauge						
Outline dimension	91.00(H)× 77.00(V) × 1.1(D)	Unit: mm	Part-A	Active area	Part-B	Border area
Environment	Temperature	Humidity	Illuminance	Distance	Time	Angle
	19℃~25℃	55%±5%RH	800~1300Lux	300 mm	35Sec	
Defect type	Inspection method	Standard		Part-A	Part-B	
Spot	Electric Display	D≤0.25 mm		Ignore	Ignore	
		0.25 mm<D≤0.4 mm		N≤4	Ignore	
		D>0.4 mm		Not Allow	Ignore	
Display unwork	Electric Display	Not Allow		Not Allow	Ignore	
Display error	Electric Display	Not Allow		Not Allow	Ignore	
Scratch or line defect(include dirt)	Visual/Film card	L≤2 mm,W≤0.2 mm		Ignore	Ignore	
		2.0mm<L≤5.0mm,0.2<W≤0.3mm,		N≤2	Ignore	
		L>5 mm,W>0.3 mm		Not Allow	Ignore	
PS Bubble	Visual/Film card	D≤0.2mm		Ignore	Ignore	
		0.2mm≤D≤0.35mm		N≤4	Ignore	
		D>0.35 mm		Not Allow	Ignore	
Corner /Edge chipping	Visual/Film card	X≤6mm,Y≤0.4mm, Do not affect the electrode circuit (Edge chipping) X≤1mm,Y≤1mm, Do not affect the electrode circuit((Corner chipping) Ignore				
Remark	1. Appearance defect should not cause electrical defects					
	2. Appearance defects should not cause dimensional accuracy problems					
	L=long W=wide D=point size N=Defects NO					



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Note21-1 : OQC inspection: One-time sampling plan for GB/T 2828.1-2012 , Inspection Level II, CR: AC/Re=0/1, MA=0.4, MI=0.65.

Note 21-2: Spot define: That only can be seen under White State or Dark State defects

Note 21-3: Any defect which is visible under gray pattern or transition process but invisible under black and white is disregarded.

Note 21-4: Any defect must be judged by Optical Microscope.

Note 21-5: Here is definition of the "Spot" and "Scratch or line defect"

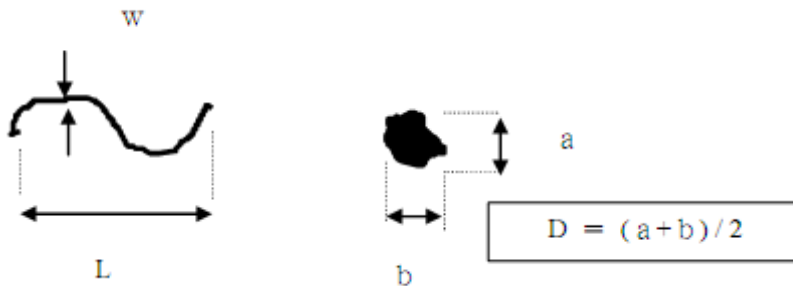
Spot: $W > 1/4L$

Scratch or line defect : $W \leq 1/4L$

Note 21-6: Definition for L/W and D (major axis)

Note 21-7: FPC bonding area pad doesn't allowed visual inspection

Note 21-8:





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22. BARCODE

22.1 label appearance



ABBBBBBBCC
DDDEEEFGGG

22.2 QR scanned information (Total 28 code number+ 2 blank spaces)

A BBBBBBBB CC DDD EEE F GGG H III J KKK
 ① ② ③ ④ ⑤ ⑥ ⑦ ⑧ ⑨ ⑩ ⑪

- ① A——The factory code
- ② BBBBBBBB——Module name of EPD
- ③ CC——FPL model name
- ④ DDD——Date of production
- ⑤ EEE——Production lot
- ⑥ F——Separator
- ⑦ GGG——FPL Lot
- ⑧ H——Normal Lot
- ⑨ III——TFT、PS、EC.
- ⑩ J——IC
- ⑪ KKK——Serial NO.
- blank spaces



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23. PACKING

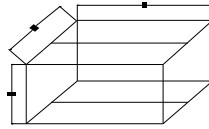
Packing Spec

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一, Package Type: Box

Box No	Holitech shipping box
Box size	515*322*170
Containment	96PCS

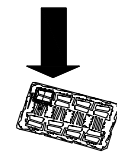


PRODUCT DRAWING



二, Inside package type: Plastic Tray
Tray unit: mm

Plastic Tray	465*280*15	13 pcs
Anti-static foil bags	700*530*0.1	1 pcs
EPE (inside)	88*221.5*2	48 pcs
EPE (Up-Down)	485*145*10	2 pcs
EPE (Left-Right)	285*480*10	2 pcs
EPE (Front-back)	310*145*10	2 pcs
Chip board	500*306*5	2 pcs
Quantity/tray	8 pcs	
Tray number/sheet	12+1 Sheets	
Box	1	



Empty tray
Anti-static EPE

Step 1:

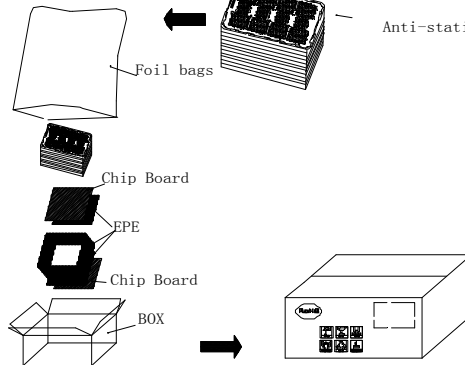
Material: Tray, EPE
Put the product in to the tray and keep the display side up. Then put anti-static EPE in to each holes.

Step 2:

1) Must keep the angle 180 degree placed between the neighboring Plastic trays.
2) There are 12 layers product, total 8*12=96 pcs.
3) An empty Plastic tray intersects put on the top of the plastic trays.

Step 3:

1) In each case, put 2 bags of desiccant, then seal the trays with adhesive tapes.
2) Put the trays into foil bags.
3) heat seal the foil bags.



Step 4:

1) First put a chip board on the bottom of the box, then placed the down EPE, the left - right and front -back EPE.
2) Placed the sealed products into the box.
3) The last placed the up EPE on the top of the trays, and place a chip board on it.

Step 5:

1) Seal the box with adhesive tapes .
2) Paste the lable onto the exterior box, and the lable can't cover the safety , transfer and RoSH sign.

Design	X. Z. P	Approve	H. Z. P	Confirm	X.X.M
Date	2020. 11. 03	Date	2020. 11. 03	Date	2020. 11. 03



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The label outside the carton print as below

90.00	
Label	
Customer Part No	
Customers Item No	A
MFG order No	B
MFG batch No	C
QTY	D
G.W	E
N.W	F
MFG Date	J
Carton No	
Remark	

NOTE:

1. "A" Print customer Item No
2. "B" Print customer Order No
3. "C" Print MFG Batch No(Separate packing for different batch products. Mixed packing available for the odd number of different batch print all the batch NO&QTY accordingly if happened.
4. "D"Print product qty
5. "E"Print the G.W
6. "F"Print the N.W
7. "J"Print the MFG date
8. Before packing make sure the FPL batch ,item and qty are the same as which on the Final passed card.

Design	X. Z. P	Approve	H. Z. P	Confirm	X.X.M
Date	2020. 11. 03	Date	2020. 11. 03	Date	2020. 11. 03