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## Specification For HINK 3.7"EPD

**Model NO: HINK-E037A39**

**Product VER:A0**

### Customer Approval

<b>Customer</b>	
<b>Approval By</b>	
<b>Date Of Approval</b>	

**It will be agreed by the receiver,if not sign back the Specification within 15days.**

<b>Prepared By</b>	<b>Checked By</b>	<b>Approval By</b>



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<b>Version</b>	<b>Content</b>	<b>Date</b>	<b>Producer</b>
A0	New release	2022/8/9	Eddie



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## 1. General Description

HINK-E037A39 is an Active Matrix Electrophoretic Display (AMEPD), with interface and a reference system design. The 3.7" active area contains 240×416 pixels, and has 1-bit B/W/R full display capabilities. An integrated circuit contains gate buffer, source buffer, interface, timing control logic, oscillator, DC-DC, SRAM, LUT, VCOM and border are supplied with each panel.

## 2. Features

- 240×416 pixels display
- High contrast
- High reflectance
- Ultra wide viewing angle
- Ultra low power consumption
- Pure reflective mode
- Bi-stable display
- Commercial temperature range
- Landscape, portrait modes
- Hard-coat antiglare display surface
- Ultra Low current deep sleep mode
- On chip display RAM
- Low voltage detect for supply voltage
- High voltage ready detect for driving voltage
- Internal temperature sensor
- 10-byte OTP space for module identification
- Waveform stored in On-chip OTP
- Serial peripheral interface available
- On-chip oscillator
- On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage
- I2C signal master interface to read external temperature sensor/ built-in temperature sensor

## 3. Application

Electronic Shelf Label System

## 4. Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	3.7	Inch	
Display Resolution	240(H)×416(V)	Pixel	Dpi:129
Active Area	47.04(H)×81.54(V)	mm	
Pixel Pitch	0.202×0.203	mm	
Pixel Configuration	Rectangle		
Outline Dimension	53(H)×92.99 (V) ×0.95(D)	mm	Without mask
Weight	8.5±0.2	g	



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### 5. Mechanical Drawing of EPD module

**HSF FRONT VIEW**

**SIDE VIEW**

**BOTTOM VIEW**

**NOTES:**

1. DISPLAY MODULE 3.7" ARRAY FOR EPD;
2. DRIVE IC: UC8253C;
3. RESOLUTION: 416gate X 240source;
4. pixel size: 0.202mm X 0.203mm;
5. Unspecified Tolerance: ±0.20;
6. Material conform to the ROHS2.0 standard
7. \* as the focus control size

Signature		Date	
A0 confirmed			

REV	DESCRIPTION	REVISOR	DATE
A0	First release	ZZQ	22.8.9

 <b>Jiangxi Xingtai Technology Co., Ltd</b>		<b>PROJECTION</b> 	
ALL UNITS: mm	DATE	MODEL NUMBER:	SHEET I:
DESIGN:ZZQ	22.8.9	HINK-E037A39-A0	DATE:22.8.9
CHK:	Ps:	1001 (1007YQ8S1)	
APP:	PN		

PIN	SIGNAL
B.P	BONDING PIN
1	NC
2	GDR
3	RESF
4	NC
5	VDHR
6	TSCL
7	TSDA
8	BS
9	BUSY_N
10	RST_N
11	DC
12	CSB
13	SCL
14	SDA
15	VDDO
16	VDD
17	GND
18	VDDD
19	VBP
20	VDHLVSH
21	VGH
22	VDL(VSL)
23	VGI
24	VCOM



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## 6. Input/Output Terminals

Pin #	Single	Description	Remark
	B.P	BONDING PIN	
1	NC	No connection and do not connect with other NC pins	Keep Open
2	GDR	N-Channel MOSFET Gate Drive Control	
3	RESE	Current Sense Input for the Control Loop	
4	NC	No connection and do not connect with other NC pins	Keep Open
5	VDHR	Positive Source driving voltage	
6	TSCL	I2C Interface to digital temperature sensor Clock pin	
7	TSDA	I2C Interface to digital temperature sensor Date pin	
8	BS	Bus selection pin	Note 6-5
9	BUSY_N	Busy state output pin	Note 6-4
10	RST_N	Reset	Note 6-3
11	DC	Data /Command control pin	Note 6-2
12	CSB	Chip Select input pin	Note 6-1
13	SCL	serial clock pin (SPI)	
14	SDA	serial data pin (SPI)	
15	VDDIO	Power for interface logic pins	
16	VDD	Power Supply pin for the chip	
17	GND	Ground	
18	VDDD	Core logic power pin	
19	VPP	Power Supply for OTP Programming	
20	VDH(VSH)	Positive source driver Voltage	
21	VGH	Positive Gate driving voltage	
22	VDL(VSL)	Negative Source driving voltage	
23	VGL	Negative Gate voltage.	
24	VCOM	VCOM driving voltage	

Note 6-1: This pin (CSB) is the chip select input connecting to the MCU. The chip is enabled for MCU communication: only when CSB is pulled LOW.

Note 6-2: This pin (DC) is Data/Command control pin connecting to the MCU. When the pin is pulled HIGH, the data will be interpreted as data. When the pin is pulled LOW, the data will be interpreted as command.

Note 6-3: This pin (RST\_N) is reset signal input. The Reset is active low.



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Note 6-4: This pin (BUSY\_N) is Busy state output pin. When Busy\_N is Low the operation of chip should not be interrupted and any commands should not be issued to the module. The driver IC will put Busy\_N pin Low when the driver IC is working such as:

- Outputting display waveform; or
- Communicating with digital temperature sensor

Note 6-5: This pin (BS) is for 3-line SPI or 4-line SPI selection. When it is "Low", 4-line SPI is selected. When it is "High", 3-line SPI (9 bits SPI) is selected.



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## 7. Host interfaces

HT0001 provides 3-wire/4-wire serial interface for command and display data transferred from the MCU. The serial interface supports 8-bit mode. Data can be input/output by clocks while the chip is active (CSB =LOW). While input, data are written in order from MSB at the clock rising edge. When too many parameters are input, the chip accepts only defined parameters, and ignores undefined ones.

BS	Interface	CSB	DC	SCL	SDA
High	3-wire SPI	Available	Fix to GND	Available	Available
Low	4-wire SPI	Available	Available	Available	Available

### 3 wire SPI format

Data / Command is recognized with the first bit transferred. Data are transferred in the unit of 9 bits. To prevent malfunction due to noise, it is recommended to set the CSB signal to HIGH every 9 bits. (The serial counter is reset at the rising edge of the CSB signal.)

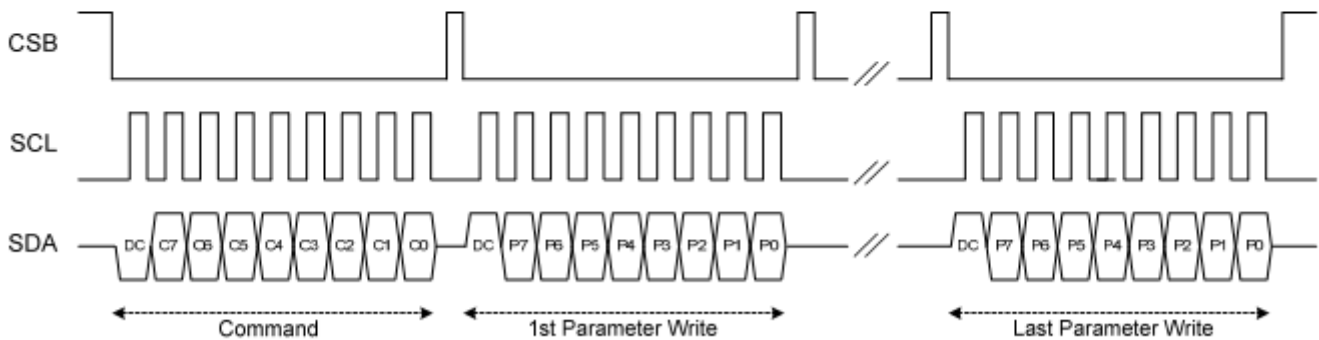


Figure: 3-wire SPI write operation

The MSB bit of data will be output at SDA pin after the 1<sup>st</sup> SCL falling edge, if the 1<sup>st</sup> input data at SDA is high.

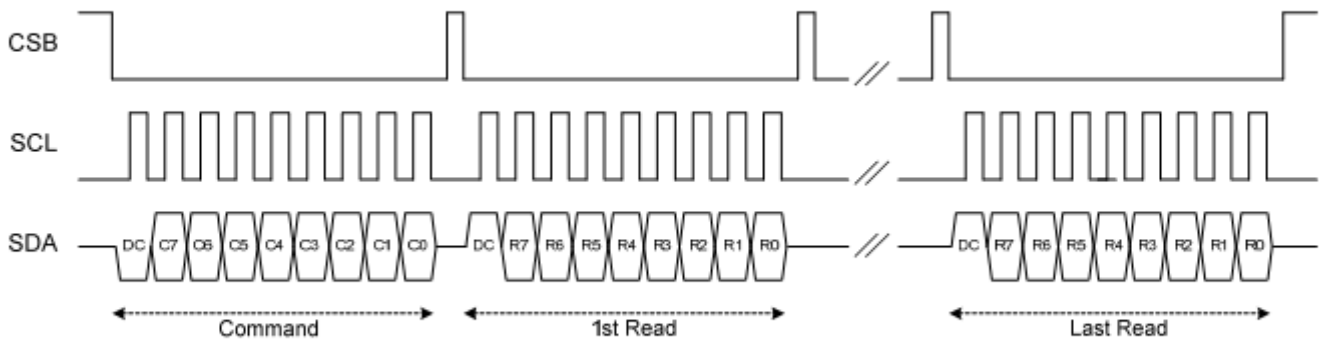


Figure: 3-wire SPI read operation





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### 4 wire SPI format

Data / Command is recognized with DC pin. Data are transferred in the unit of 8 bits. To prevent malfunction due to noise, it is recommended to set the CSB signal to HIGH every 8 bits. (The serial counter is reset at the rising edge of the CSB signal.)

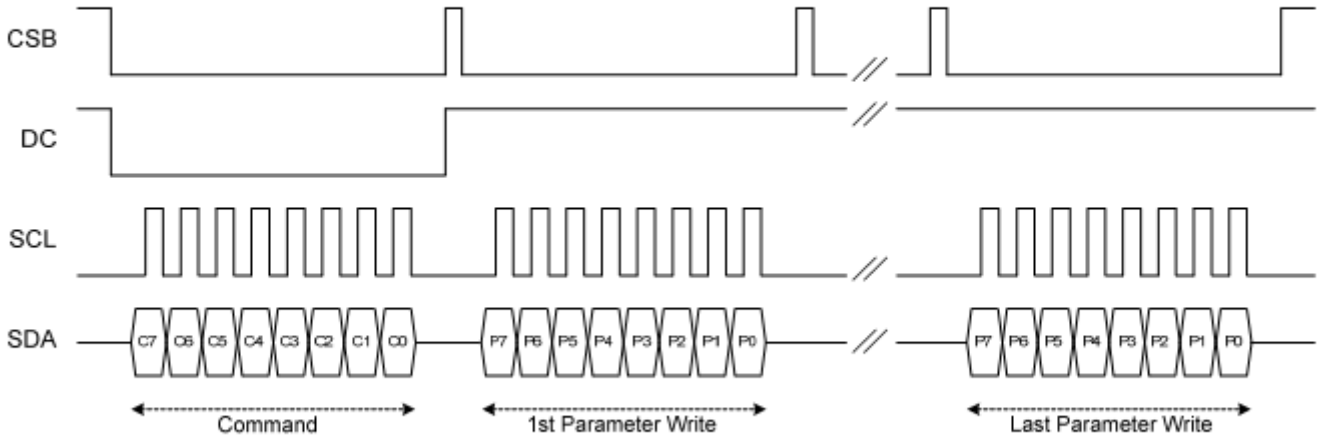


Figure: 4-wire SPI write operation

The MSB bit of data will be output at SDA pin after the CSB falling edge, if DC pin is High.

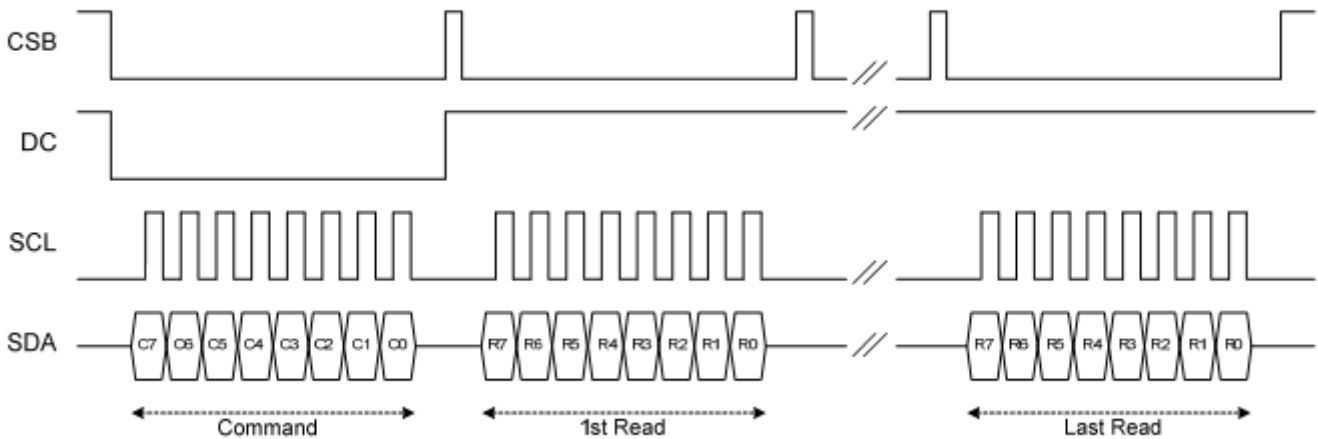


Figure: 4-wire SPI read operation



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## 8. Temperature sensor operation

Following is the way of how to sense the ambient temperature of the module. First, use an external temperature sensor to get the temperature value and converted it into HEX format with below mapping table, then send command 0x1A with the HEX temperature value to the module thru the SPI interface.

The temperature value to HEX conversion is as follow:

1. If the Temperature value MSByte bit D11 = 0, then

The temperature is positive and value (DegC) = + (Temperature value) / 16

2. If the Temperature value MSByte bit D11 = 1, then

The temperature is negative and value (DegC) = ~ (2's complement of Temperature value) / 16

12-bit binary (2's complement)	Hexadecimal Value	Decimal Value	Value [DegC]
0111 1111 0000	7F0	2032	127
0111 1110 1110	7EE	2030	126.875
0111 1110 0010	7E2	2018	126.125
0111 1101 0000	7D0	2000	125
0001 1001 0000	190	400	25
0000 0000 0010	002	2	0.125
0000 0000 0000	000	0	0
1111 1111 1110	FFE	-2	-0.125
1110 0111 0000	E70	-400	-25
1100 1001 0010	C92	-878	-54.875
1100 1001 0000	C90	-880	-55



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## 9. COMMAND TABLE

W/R: 0: Write Cycle 1: Read Cycle    C/D: 0: Command / 1: Data    D7~D0: -: Don't Care #: Valid Data

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default	
1	Panel Setting (PSR)	0	0	0	0	0	0	0	0	0	0		00H	
		0	1	--	--	#	#	#	#	#	#		REG, KW/R, UD, SHL, SHD_N, RST_N	0FH
2	Power Setting (PWR)	0	0	0	0	0	0	0	0	0	1		01H	
		0	1	--	--	--	--	--	#	#	#		VSR_EN, VS_EN, VG_EN	03H
		0	1	--	--	--	--	#	#	#	#		VCOM_HV, VG_LVL[2:0]	00H
		0	1	--	--	#	#	#	#	#	#		VDH_LVL[5:0]	3FH
		0	1	--	--	#	#	#	#	#	#		VDL_LVL[5:0]	3FH
0	1	--	--	#	#	#	#	#	#		VDHR_LVL[5:0]	0DH		
3	Power OFF (POF)	0	0	0	0	0	0	0	0	1	0		02H	
4	Power OFF Sequence Setting (PFS)	0	0	0	0	0	0	0	0	1	1		03H	
		0	1	--	--	#	#	--	--	--	--		T_VDS_OFF[1:0]	00H
5	Power ON (PON)	0	0	0	0	0	0	0	1	0	0		04H	
6	Power ON Measure (PMES)	0	0	0	0	0	0	0	1	0	1		05H	
7	Booster Soft Start (BTST)	0	0	0	0	0	0	0	1	1	0		06H	
		0	1	#	#	#	#	#	#	#	#		BT_PHA[7:0]	17H
		0	1	#	#	#	#	#	#	#	#		BT_PHB[7:0]	17H
		0	1	--	--	#	#	#	#	#	#		BT_PHC[5:0]	17H
8	Deep sleep (DSLSP)	0	0	0	0	0	0	0	1	1	1		07H	
		0	1	1	0	1	0	0	1	0	1		Check code	A5H
9	Display Start Transmission 1 (DTM1, White/Black Data) (x-byte command)	0	0	0	0	0	1	0	0	0	0	K/W or OLD Pixel Data	10H	
		0	1	#	#	#	#	#	#	#	#		KPXL[1:8]	-
		0	1	:	:	:	:	:	:	:	:		:	:
		0	1	#	#	#	#	#	#	#	#		KPXL[n-7:n]	-
10	Data Stop (DSP)	0	0	0	0	0	1	0	0	0	1		11H	
		1	1	#	--	--	--	--	--	--	--		00H	
11	Display Refresh (DRF)	0	0	0	0	0	1	0	0	1	0		12H	
12	Display Start transmission 2 (DTM2, Red Data) (x-byte command)	0	0	0	0	0	1	0	0	1	1	Red or NEW Pixel Data	13H	
		0	1	#	#	#	#	#	#	#	#		RPXL[1:8]	-
		0	1	:	:	:	:	:	:	:	:		:	:
		0	1	#	#	#	#	#	#	#	#		RPXL[n-7:n]	-
13	Auto Sequence (AUTO)	0	0	0	0	0	1	0	1	1	1		17H	
		0	1	1	0	1	0	0	1	0	1		Check code	A5H
14	VCOM LUT (LUTC) (61-byte command, structure of bytes 2~7 repeated 10 times)	0	0	0	0	1	0	0	0	0	0		20H	
		0	1	#	#	#	#	#	#	#	#		Level select-0~3[1:0]	-
		0	1	:	:	:	:	:	:	:	:		Number of frames-0[7:0]	-
		0	1	:	:	:	:	:	:	:	:		Number of frames-1[7:0]	-
		0	1	:	:	:	:	:	:	:	:		Number of frames-2[7:0]	-
		0	1	:	:	:	:	:	:	:	:		Number of frames-3[7:0]	-
0	1	#	#	#	#	#	#	#	#		Times to repeat[7:0]	-		



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#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default	
15	W2W LUT (LUTWW) (43-byte command, structure of bytes 2~7 repeated 7 times)	0	0	0	0	1	0	0	0	0	1		21H	
		0	1	#	#	#	#	#	#	#	#	Level select-0~3[1:0]	-	
		0	1	:	:	:	:	:	:	:	:	:	Number of frames-0[7:0]	-
		0	1	:	:	:	:	:	:	:	:	:	Number of frames-1[7:0]	-
		0	1	:	:	:	:	:	:	:	:	:	Number of frames-2[7:0]	-
		0	1	:	:	:	:	:	:	:	:	:	Number of frames-3[7:0]	-
		0	1	#	#	#	#	#	#	#	#	Times to repeat[7:0]	-	
16	K2W LUT (LUTKW / LUTR) (61-byte command, structure of bytes 2~7 repeated 10 times)	0	0	0	0	1	0	0	0	0	1	0	22H	
		0	1	#	#	#	#	#	#	#	#	#	Level select-0~3[1:0]	-
		0	1	:	:	:	:	:	:	:	:	:	Number of frames-0[7:0]	-
		0	1	:	:	:	:	:	:	:	:	:	Number of frames-1[7:0]	-
		0	1	:	:	:	:	:	:	:	:	:	Number of frames-2[7:0]	-
		0	1	:	:	:	:	:	:	:	:	:	Number of frames-3[7:0]	-
		0	1	#	#	#	#	#	#	#	#	Times to repeat[7:0]	-	
17	W2K LUT (LUTWK / LUTW) (61-byte command, structure of bytes 2~7 repeated 10 times)	0	0	0	0	1	0	0	0	0	1	1	23H	
		0	1	#	#	#	#	#	#	#	#	#	Level select-0~3[1:0]	-
		0	1	:	:	:	:	:	:	:	:	:	Number of frames-0[7:0]	-
		0	1	:	:	:	:	:	:	:	:	:	Number of frames-1[7:0]	-
		0	1	:	:	:	:	:	:	:	:	:	Number of frames-2[7:0]	-
		0	1	:	:	:	:	:	:	:	:	:	Number of frames-3[7:0]	-
		0	1	#	#	#	#	#	#	#	#	Times to repeat[7:0]	-	
18	K2K LUT (LUTKK / LUTK) (61-byte command, structure of bytes 2~7 repeated 10 times)	0	0	0	0	1	0	0	0	1	0	0	24H	
		0	1	#	#	#	#	#	#	#	#	#	Level select-0~3[1:0]	-
		0	1	:	:	:	:	:	:	:	:	:	Number of frames-0[7:0]	-
		0	1	:	:	:	:	:	:	:	:	:	Number of frames-1[7:0]	-
		0	1	:	:	:	:	:	:	:	:	:	Number of frames-2[7:0]	-
		0	1	:	:	:	:	:	:	:	:	:	Number of frames-3[7:0]	-
		0	1	#	#	#	#	#	#	#	#	Times to repeat[7:0]	-	
19	LUT option (LUTOPT)	0	0	0	0	1	0	1	0	1	0		2AH	
		0	1	#	#	--	--	--	--	--	--	STATE_XON[9:8]	00H	
		0	1	#	#	#	#	#	#	#	#	#	STATE_XON[7:0]	00H
20	PLL control (PLL)	0	0	0	0	1	1	0	0	0	0		30H	
		0	1	--	--	--	--	#	#	#	#	FRS[3:0]	04H	
21	Temperature Sensor Calibration (TSC)	0	0	0	1	0	0	0	0	0	0		40H	
		1	1	#	#	#	#	#	#	#	#	D[10:3] / TS[7:0]	00H	
		1	1	#	#	#	--	--	--	--	--	--	D[2:0] / -	00H
22	Temperature Sensor Selection (TSE)	0	0	0	1	0	0	0	0	0	1		41H	
		0	1	#	--	--	--	#	#	#	#	TSE, TO[3:0]	00H	
23	Temperature Sensor Write (TSW)	0	0	0	1	0	0	0	0	0	1	0	42H	
		0	1	#	#	#	#	#	#	#	#	#	WATTR[7:0]	00H
		0	1	#	#	#	#	#	#	#	#	#	WMSB[7:0]	00H
		0	1	#	#	#	#	#	#	#	#	#	WLSB[7:0]	00H
24	Temperature Sensor Read (TSR)	0	0	0	1	0	0	0	0	0	1	1	43H	
		1	1	#	#	#	#	#	#	#	#	#	RMSB[7:0]	00H
		1	1	#	#	#	#	#	#	#	#	RLSB[7:0]	00H	



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#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default	
25	Panel Break Check (PBC)	0	0	0	1	0	0	0	1	0	0		44H	
		1	1	--	--	--	--	--	--	--	#	PSTA	00H	
26	VCOM and data interval setting (CDI)	0	0	0	1	0	1	0	0	0	0		50H	
		0	1	#	--	#	#	--	--	#	#	BDZ, BDV[1:0], DDX[1:0]	31H	
		0	1	--	--	--	--	#	#	#	#	CDI[3:0]	07H	
27	Lower Power Detection (LPD)	0	0	0	1	0	1	0	0	0	1		51H	
		1	1	--	--	--	--	--	--	--	#	LPD	01H	
28	TCON setting (TCON)	0	0	0	1	1	0	0	0	0	0		60H	
		0	1	#	#	#	#	#	#	#	#	S2G[3:0], G2S[3:0]	22H	
29	Resolution setting (TRES)	0	0	0	1	1	0	0	0	0	1		61H	
		0	1	#	#	#	#	#	0	0	0	HRES[7:3]	F0H	
		0	1	--	--	--	--	--	--	#	#	VRES[9:0]	02H	
		0	1	#	#	#	#	#	#	#	#		00H	
30	Gate/Source Start setting (GSST)	0	0	0	1	1	0	0	1	0	1		65H	
		0	1	#	#	#	#	#	0	0	0	HST[7:3]	00H	
		0	1	--	--	--	--	--	--	--	#	VST[8:0]	00H	
		0	1	#	#	#	#	#	#	#	#		00H	
31	Revision (REV)	0	0	0	1	1	1	0	0	0	0		70H	
		1	1	#	#	#	#	#	#	#	#	LUT_REV[7:0]	FFH	
32	Get Status (FLG)	0	0	0	1	1	1	0	0	0	1		71H	
		1	1	--	#	#	#	#	#	#	#	PTL_FLAG, I <sup>2</sup> C_ERR, I <sup>2</sup> C_BUSYN, DATA_FLAG, PON, POF, BUSY_N	13H	
33	Auto Measurement VCOM (AMV)	0	0	1	0	0	0	0	0	0	0		80H	
		0	1	--	--	#	#	#	#	#	#	AMVT[1:0], XON, AMVS, AMV, AMVE	10H	
34	Read VCOM Value (VV)	0	0	1	0	0	0	0	0	0	1		81H	
		1	1	--	--	#	#	#	#	#	#	VV[5:0]	00H	
35	VCOM_DC Setting (VDCS)	0	0	1	0	0	0	0	0	1	0		82H	
		0	1	--	--	#	#	#	#	#	#	VDCS[5:0]	00H	
36	Partial Window (PTL)	0	0	1	0	0	1	0	0	0	0		90H	
		0	1	#	#	#	#	#	0	0	0	HRST[7:3]	00H	
		0	1	#	#	#	#	#	1	1	1	HRED[7:3]	EFH	
		0	1	--	--	--	--	--	--	--	#	VRST[8:0]	00H	
		0	1	#	#	#	#	#	#	#	#		00H	
		0	1	--	--	--	--	--	--	--	#	VRED[8:0]	01H	
		0	1	#	#	#	#	#	#	#	#		FFH	
		0	1	--	--	--	--	--	--	--	#	PT_SCAN	01H	
37	Partial In (PTIN)	0	0	1	0	0	1	0	0	0	1		91H	
38	Partial Out (PTOUT)	0	0	1	0	0	1	0	0	1	0		92H	
39	Program Mode (PGM)	0	0	1	0	1	0	0	0	0	0		A0H	
40	Active Programming (APG)	0	0	1	0	1	0	0	0	0	1		A1H	
41	Read OTP (ROTP)	0	0	1	0	1	0	0	0	1	0		A2H	
		1	1	#	#	#	#	#	#	#	#	Data of Address = 000h	N/A	
		1	1	:	:	:	:	:	:	:	:	:	:	N/A
		1	1	#	#	#	#	#	#	#	#	Data of Address = n	N/A	
42	Cascade Setting (CCSET)	0	0	1	1	1	0	0	0	0	0		E0H	
		0	1	--	--	--	--	--	--	--	#	#	TSFIX, CCEN	00H



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#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
43	Power Saving (PWS)	0	0	1	1	1	0	0	0	1	1		E3H
		0	1	#	#	#	#	#	#	#	#	VCOM_W[3:0], SD_W[3:0]	00H
44	LVD Voltage Select (LVSEL)	0	0	1	1	1	0	0	1	0	0		E4H
		0	1	--	--	--	--	--	--	#	#	LVD_SEL[1:0]	03H
45	Force Temperature (TSSET)	0	0	1	1	1	0	0	1	0	1		E5H
		0	1	#	#	#	#	#	#	#	#	TS_SET[7:0]	00H

- Note:** (1) All other register addresses are invalid or reserved, and should NOT be used.  
 (2) Any bits shown here as 0 must be written with a 0. All unused bits should also be set to zero. Device malfunction may occur if this is not done.  
 (3) Commands are processed on the 'stop' condition of the interface.  
 (4) Registers marked 'W/R' can be read, but the contents are written when the SPI command completes – so the contents can be read and altered. The user can subsequently write the register to restore the contents following an SPI read.

## 10.COMMAND DESCRIPTION

**W/R:** 0: Write Cycle / 1: Read Cycle    **C/D:** 0: Command / 1: Data    **D7-D0:** -: Don't Care

### (1) PANEL SETTING (PSR) (REGISTER: R00H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Setting the panel	0	0	0	0	0	0	0	0	0	0
	0	1	-	-	REG	KW/R	UD	SHL	SHD_N	RST_N

- REG:** LUT selection  
 0: LUT from OTP. (Default)  
 1: LUT from register.
- KW/R:** Black / White / Red  
 0: Pixel with Black/White/Red, KWR mode. (Default)  
 1: Pixel with Black/White, KW mode.
- UD:** Gate Scan Direction  
 0: Scan down. First line to Last line: Gn-1 → Gn-2 → Gn-3 → ... → G0  
 1: Scan up. (Default) First line to Last line: G0 → G1 → G2 → ... → Gn-1
- SHL:** Source Shift Direction  
 0: Shift left. First data to Last data: Sn-1 → Sn-2 → Sn-3 → ... → S0  
 1: Shift right. (Default) First data to Last data: S0 → S1 → S2 → ... → Sn-1
- SHD\_N:** Booster Switch  
 0: Booster OFF  
 1: Booster ON (Default)  
 When SHD\_N becomes LOW, charge pump will be turned OFF, register and SRAM data will keep until VDD OFF. And Source/Gate/Border/VCOM will be released to floating.
- RST\_N:** Soft Reset  
 0: Reset. Booster OFF, Register data are set to their default values, all drivers will be reset, and all functions will be disabled. Source/Gate/Border/VCOM will be released to floating.  
 1: No effect (Default).



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**(2) POWER SETTING (PWR) (R01H)**

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Selecting Internal/External Power	0	0	0	0	0	0	0	0	0	1	01H
	0	1	-	-	-	-	-	VSR_EN	VS_EN	VG_EN	07H
	0	1	-	-	-	-	VCOM_HV	VG_LVL[2:0]			00H
	0	1	-	-	VDH_LVL[5:0]						3FH
	0	1	-	-	VDL_LVL[5:0]						3FH
	0	1	-	-	VDHR_LVL[5:0]						0DH

- VSR\_EN:** Source LV power selection  
 0 : External source power from VDHR pins  
 1 : Internal DC/DC function for generating VDHR. (Default)
- VS\_EN:** Source power selection  
 0 : External source power from VDH/VDL pins  
 1 : Internal DC/DC function for generating VDH/VDL. (Default)
- VG\_EN:** Gate power selection  
 0 : External gate power from VGH/VGL pins  
 1 : Internal DC/DC function for generating VGH/VGL. (Default)
- VCOM\_HV:** VCOM Voltage Level  
 0 : VCOMH=VDH+VCOM\_DC, VCOML=VDL+VCOM\_DC. (Default)  
 1 : VCOMH=VGH, VCOML=VGL
- VG\_LVL[2:0]:**VGH / VGL Voltage Level selection.

VG_LVL[2:0]	VGH/VGL Voltage Level
000	VGH=9V, VGL= -9V
001	VGH=10V, VGL= -10V
010	VGH=11V, VGL= -11V
011	VGH=12V, VGL= -12V
100	VGH=17V, VGL= -17V
101	VGH=18V, VGL= -18V
110	VGH=19V, VGL= -19V
111 (Default)	VGH=20V, VGL= -20V

**VDH\_LVL[5:0]:** Internal VDH power selection for K/W pixel. (Default value: 11 1111b)

VDH_LVL	Voltage	VDH_LVL	Voltage	VDH_LVL	Voltage	VDH_LVL	Voltage
000000	2.4 V	010001	5.8 V	100010	9.2 V	110011	12.6 V
000001	2.6 V	010010	6.0 V	100011	9.4 V	110100	12.8 V
000010	2.8 V	010011	6.2 V	100100	9.6 V	110101	13.0 V
000011	3.0 V	010100	6.4 V	100101	9.8 V	110110	13.2 V
000100	3.2 V	010101	6.6 V	100110	10.0 V	110111	13.4 V
000101	3.4 V	010110	6.8 V	100111	10.2 V	111000	13.6 V
000110	3.6 V	010111	7.0 V	101000	10.4 V	111001	13.8 V
000111	3.8 V	011000	7.2 V	101001	10.6 V	111010	14.0 V
001000	4.0 V	011001	7.4 V	101010	10.8 V	111011	14.2 V
001001	4.2 V	011010	7.6 V	101011	11.0 V	111100	14.4 V
001010	4.4 V	011011	7.8 V	101100	11.2 V	111101	14.6 V
001011	4.6 V	011100	8.0 V	101101	11.4 V	111110	14.8 V
001100	4.8 V	011101	8.2 V	101110	11.6 V	111111	15.0 V
001101	5.0 V	011110	8.4 V	101111	11.8 V		
001110	5.2 V	011111	8.6 V	110000	12.0 V		
001111	5.4 V	100000	8.8 V	110001	12.2 V		
010000	5.6 V	100001	9.0 V	110010	12.4 V		



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**VDL\_LVL[5:0]:** Internal VDL power selection for K/W pixel. (Default value: 11 1111b)

VDL_LVL	Voltage	VDL_LVL	Voltage	VDL_LVL	Voltage	VDL_LVL	Voltage
000000	-2.4 V	010001	-5.8 V	100010	-9.2 V	110011	-12.6 V
000001	-2.6 V	010010	-6.0 V	100011	-9.4 V	110100	-12.8 V
000010	-2.8 V	010011	-6.2 V	100100	-9.6 V	110101	-13.0 V
000011	-3.0 V	010100	-6.4 V	100101	-9.8 V	110110	-13.2 V
000100	-3.2 V	010101	-6.6 V	100110	-10.0 V	110111	-13.4 V
000101	-3.4 V	010110	-6.8 V	100111	-10.2 V	111000	-13.6 V
000110	-3.6 V	010111	-7.0 V	101000	-10.4 V	111001	-13.8 V
000111	-3.8 V	011000	-7.2 V	101001	-10.6 V	111010	-14.0 V
001000	-4.0 V	011001	-7.4 V	101010	-10.8 V	111011	-14.2 V
001001	-4.2 V	011010	-7.6 V	101011	-11.0 V	111100	-14.4 V
001010	-4.4 V	011011	-7.8 V	101100	-11.2 V	111101	-14.6 V
001011	-4.6 V	011100	-8.0 V	101101	-11.4 V	111110	-14.8 V
001100	-4.8 V	011101	-8.2 V	101110	-11.6 V	111111	-15.0 V
001101	-5.0 V	011110	-8.4 V	101111	-11.8 V		
001110	-5.2 V	011111	-8.6 V	110000	-12.0 V		
001111	-5.4 V	100000	-8.8 V	110001	-12.2 V		
010000	-5.6 V	100001	-9.0 V	110010	-12.4 V		

**VDHR\_LVL[5:0]:** Internal VDHR power selection for Red pixel. (Default value: 00 1101b)

VDHR_LVL	Voltage	VDHR_LVL	Voltage	VDHR_LVL	Voltage	VDHR_LVL	Voltage
000000	2.4 V	010001	5.8 V	100010	9.2 V	110011	12.6 V
000001	2.6 V	010010	6.0 V	100011	9.4 V	110100	12.8 V
000010	2.8 V	010011	6.2 V	100100	9.6 V	110101	13.0 V
000011	3.0 V	010100	6.4 V	100101	9.8 V	110110	13.2 V
000100	3.2 V	010101	6.6 V	100110	10.0 V	110111	13.4 V
000101	3.4 V	010110	6.8 V	100111	10.2 V	111000	13.6 V
000110	3.6 V	010111	7.0 V	101000	10.4 V	111001	13.8 V
000111	3.8 V	011000	7.2 V	101001	10.6 V	111010	14.0 V
001000	4.0 V	011001	7.4 V	101010	10.8 V	111011	14.2 V
001001	4.2 V	011010	7.6 V	101011	11.0 V	111100	14.4 V
001010	4.4 V	011011	7.8 V	101100	11.2 V	111101	14.6 V
001011	4.6 V	011100	8.0 V	101101	11.4 V	111110	14.8 V
001100	4.8 V	011101	8.2 V	101110	11.6 V	111111	15.0 V
001101	5.0 V	011110	8.4 V	101111	11.8 V		
001110	5.2 V	011111	8.6 V	110000	12.0 V		
001111	5.4 V	100000	8.8 V	110001	12.2 V		
010000	5.6 V	100001	9.0 V	110010	12.4 V		

### (3) POWER OFF (POF) (R02H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Turning OFF the power	0	0	0	0	0	0	0	0	1	0

After the Power OFF command, the driver will be powered OFF. Refer to the POWER MANAGEMENT section for the sequence.

This command will turn off booster, controller, source driver, gate driver, VCOM, and temperature sensor, but register data will be kept until VDD turned OFF or Deep Sleep Mode. Source/Gate/Border/VCOM will be released to floating.

### (4) POWER OFF SEQUENCE SETTING (PFS) (R03H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Setting Power OFF sequence	0	0	0	0	0	0	0	0	1	1
	0	1	-	-	T_VDS_OFF[1:0]	-	-	-	-	-

**T\_VDS\_OFF[1:0]:** Source to gate power off interval time.

00b: 1 frame (Default)

01b: 2 frames

10b: 3 frames

11b: 4 frame





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### (5) POWER ON (PON) (REGISTER: R04H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Turning ON the power	0	0	0	0	0	0	0	1	0	0	04H

After the Power ON command, the driver will be powered ON. Refer to the POWER MANAGEMENT section for the sequence.

This command will turn on booster, controller, regulators, and temperature sensor will be activated for one-time sensing before enabling booster. When all voltages are ready, the BUSY\_N signal will return to high.

### (6) POWER ON MEASURE (PMES) (R05H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
	0	0	0	0	0	0	0	1	0	1	05H

This command enables the internal bandgap, which will be cleared by the next POF.

### (7) BOOSTER SOFT START (BTST) (R06H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Starting data transmission	0	0	0	0	0	0	0	1	1	0	06H
	0	1	BT_PHA[7:6]			BT_PHA[5:3]		BT_PHA[2:0]			17H
	0	1	BT_PHB[7:6]			BT_PHB[5:3]		BT_PHB[2:0]			17H
	0	1	-	-	BT_PHC[5:3]		BT_PHC[2:0]			17H	

**BT\_PHA[7:6]:** Soft start period of phase A.

00b: 10mS      01b: 20mS      10b: 30mS      11b: 40mS

**BT\_PHA[5:3]:** Driving strength of phase A

000b: strength 1      001b: strength 2      010b: strength 3      011b: strength 4  
100b: strength 5      101b: strength 6      110b: strength 7      111b: strength 8 (strongest)

**BT\_PHA[2:0]:** Minimum OFF time setting of GDR in phase A

000b: 0.27uS      001b: 0.34uS      010b: 0.40uS      011b: 0.54uS  
100b: 0.80uS      101b: 1.54uS      110b: 3.34uS      111b: 6.58uS

**BT\_PHB[7:6]:** Soft start period of phase B.

00b: 10mS      01b: 20mS      10b: 30mS      11b: 40mS

**BT\_PHB[5:3]:** Driving strength of phase B

000b: strength 1      001b: strength 2      010b: strength 3      011b: strength 4  
100b: strength 5      101b: strength 6      110b: strength 7      111b: strength 8 (strongest)

**BT\_PHB[2:0]:** Minimum OFF time setting of GDR in phase B

000b: 0.27uS      001b: 0.34uS      010b: 0.40uS      011b: 0.54uS  
100b: 0.80uS      101b: 1.54uS      110b: 3.34uS      111b: 6.58uS

**BT\_PHC[5:3]:** Driving strength of phase C

000b: strength 1      001b: strength 2      010b: strength 3      011b: strength 4  
100b: strength 5      101b: strength 6      110b: strength 7      111b: strength 8 (strongest)

**BT\_PHC[2:0]:** Minimum OFF time setting of GDR in phase C

000b: 0.27uS      001b: 0.34uS      010b: 0.40uS      011b: 0.54uS  
100b: 0.80uS      101b: 1.54uS      110b: 3.34uS      111b: 6.58uS



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**(8) DEEP SLEEP (DSLPL) (R07H)**

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Deep Sleep	0	0	0	0	0	0	0	1	1	1
	0	1	1	0	1	0	0	1	0	1

After this command is transmitted, the chip will enter Deep Sleep Mode to save power. Deep Sleep Mode will return to Standby Mode by hardware reset. The only one parameter is a check code, the command will be executed if check code = 0xA5.

**(9) DATA START TRANSMISSION 1 (DTM1) (R10H)**

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Starting data transmission	0	0	0	0	0	1	0	0	0	0
	0	1	Pixel1	Pixel2	Pixel3	Pixel4	Pixel5	Pixel6	Pixel7	Pixel8
	0	1	:	:	:	:	:	:	:	:
	0	1	Pixel(n-7)	Pixel(n-6)	Pixel(n-5)	Pixel(n-4)	Pixel(n-3)	Pixel(n-2)	Pixel(n-1)	Pixel(n)

This command starts transmitting data and write them into SRAM.

In KW mode, this command writes "OLD" data to SRAM.

In KWR mode, this command writes "KW" data to SRAM.

In Program mode, this command writes "OTP" data to SRAM for programming.

**(10) DATA STOP (DSP) (R11H)**

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Stopping data transmission	0	0	0	0	0	1	0	0	0	1
	1	1	data_flag	-	-	-	-	-	-	-

Check the completeness of data. If data is complete, start to refresh display.

**Data\_flag:** Data flag of receiving user data.

0: Driver didn't receive all the data.

1: Driver has already received all the one-frame data (DTM1 and DTM2).

After "Data Start" (R10h) or "Data Stop" (R11h) commands and when data\_flag=1, the refreshing of panel starts and BUSY\_N signal will become "0".

**(11) DISPLAY REFRESH (DRF) (R12H)**

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Refreshing the display	0	0	0	0	0	1	0	0	1	0

While user sent this command, driver will refresh display (data/VCOM) according to SRAM data and LUT.

After Display Refresh command, BUSY\_N signal will become "0" and the refreshing of panel starts.



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**(12) DATA START TRANSMISSION 2 (DTM2) (R13H)**

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Starting data transmission	0	0	0	0	0	1	0	0	1	1
	0	1	Pixel1	Pixel2	Pixel3	Pixel4	Pixel5	Pixel6	Pixel7	Pixel8
	0	1	:	:	:	:	:	:	:	:
	0	1	Pixel(n-7)	Pixel(n-6)	Pixel(n-5)	Pixel(n-4)	Pixel(n-3)	Pixel(n-2)	Pixel(n-1)	Pixel(n)

This command starts transmitting data and write them into SRAM.

In KW mode, this command writes "NEW" data to SRAM.

In KWR mode, this command writes "RED" data to SRAM.

**(13) AUTO SEQUENCE (AUTO) (R17H)**

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Auto Sequence	0	0	0	0	0	1	0	1	1	1
	0	1	1	0	1	0	0	1	0	1

The command can enable the internal sequence to execute several commands continuously. The successive execution can minimize idle time to avoid unnecessary power consumption and reduce the complexity of host's control procedure. The sequence contains several operations, including PON, DRF, POF, DSLP.

AUTO (0x17) + Code(0xA5) = (PON → DRF → POF)

AUTO (0x17) + Code(0xA7) = (PON → DRF → POF → DSLP)



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**(14) VCOM LUT (LUTC) (R20H)**

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Build Look-up Table for VCOM (61-byte command, structure of bytes 2~7 repeated 10 times)	0	0	0	0	1	0	0	0	0	0
	0	1	LEVEL SELECT-0	LEVEL SELECT-1	LEVEL SELECT-2	LEVEL SELECT-3				
	0	1	NUMBER OF FRAMES-0							
	0	1	NUMBER OF FRAMES-1							
	0	1	NUMBER OF FRAMES-2							
	0	1	NUMBER OF FRAMES-3							
	0	1	TIMES TO REPEAT							

This command stores VCOM Look-Up Table with 10 groups of data. Each group contains information for one state and is stored with 6 bytes (byte 2~7, 8~13, 14~19, 20~25, ...), while the sixth byte indicates how many times that phase will repeat.

**Bytes 2, 8, 14, 20, 26, 32, 38, 44, 50, 56:**

D[7:6], D[5:4], D[3:2], D[1:0]: Level Selection

- 00b: VCOM\_DC
- 01b: VDH+VCOM\_DC (VCOMH)
- 10b: VDL+VCOM\_DC (VCOML)
- 11b: Floating

**Bytes 3~6, 9~12, 15~18, 21~24, 27~30, 33~36, 39~42, 45~48, 51~54, 57~60:**

Number of Frames

0000 0000b: 0 frame

:  
:

1111 1111b: 255 frames

**Bytes 7, 13, 19, 25, 31, 37, 43, 49, 55, 61:**

Times to Repeat

0000 0000b: 0 time

:  
:

1111 1111b: 255 times

If KW/R=0 (KWR mode), all 10 groups are used.

If KW/R=1 (KW mode), only 7 groups are used.



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**(15) W2W LUT (LUTWW) (R21H)**

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Build White Look-up Table for W2W (43-byte command, structure of bytes 2~7 repeated 7 times)	0	0	0	0	1	0	0	0	0	1
	0	1	LEVEL SELECT-0	LEVEL SELECT-1	LEVEL SELECT-2	LEVEL SELECT-3				
	0	1	NUMBER OF FRAMES-0							
	0	1	NUMBER OF FRAMES-1							
	0	1	NUMBER OF FRAMES-2							
	0	1	NUMBER OF FRAMES-3							
	0	1	TIMES TO REPEAT							

This command stores White-to-White Look-Up Table with 7 groups of data. Each group contains information for one state and is stored with 6 bytes (byte 2~7, 8~13, 14~19, 20~25, ...), while the sixth byte indicates how many times that phase will repeat.

**Bytes 2, 8, 14, 20, 26, 32, 38:**

Level Selection.

- 00b: GND
- 01b: VDH
- 10b: VDL
- 11b: VDHR

**Bytes 3~6, 9~12, 15~18, 21~24, 27~30, 33~36, 39~42:**

Number of Frames

- 0000 0000b: 0 frame
- : :
- : :
- 1111 1111b: 255 frames

**Bytes 7, 13, 19, 25, 31, 37, 43:**

Times to Repeat

- 0000 0000b: 0 time
- : :
- : :
- 1111 1111b: 255 times

If KW/R=0 (KWR mode), LUTWW is not used.

If KW/R=1 (KW mode), LUTWW is used.



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**(16) K2W LUT (LUTKW / LUTR) (R22H)**

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Build Look-up Table for K2W or Red (61-byte command, structure of bytes 2~7 repeated 10 times)	0	0	0	0	1	0	0	0	1	0
	0	1	LEVEL SELECT-0	LEVEL SELECT-1	LEVEL SELECT-2	LEVEL SELECT-3				
	0	1	NUMBER OF FRAMES-0							
	0	1	NUMBER OF FRAMES-1							
	0	1	NUMBER OF FRAMES-2							
	0	1	NUMBER OF FRAMES-3							
	0	1	TIMES TO REPEAT							

This command stores White-to-White Look-Up Table with 10 groups of data. Each group contains information for one state and is stored with 6 bytes (byte 2~7, 8~13, 14~19, 20~25, ...), while the sixth byte indicates how many times that phase will repeat.

**Bytes 2, 8, 14, 20, 26, 32, 38, 44, 50, 56:**

Level Selection.

00b: GND  
01b: VDH  
10b: VDL  
11b: VDHR

**Bytes 3~6, 9~12, 15~18, 21~24, 27~30, 33~36, 39~42, 45~48, 51~54, 57~60:**

Number of Frames

0000 0000b: 0 frame

:  
:  
:

1111 1111b: 255 frames

**Bytes 7, 13, 19, 25, 31, 37, 43, 49, 55, 61:**

Times to Repeat

0000 0000b: 0 time

:  
:  
:

1111 1111b: 255 times

If KW/R=0 (KWR mode), all 10 groups are used.

If KW/R=1 (KW mode), only 7 groups are used.

**(17) W2K LUT (LUTWK / LUTW) (R23H)**

This command builds Look-up Table for White-to-Black. Please refer to K2W LUT (LUTKW/LUTR) for similar definition details. Regardless of KW/R=0 or KW/R=1, LUTWK/LUTW is used.

**(18) K2K LUT (LUTKK / LUTK) (R24H)**

This command builds Look-up Table for Black-to-Black. Please refer to K2W LUT (LUTKW/LUTR) for similar definition details. Regardless of KW/R=0 or KW/R=1, LUTKK/LUTK is used.



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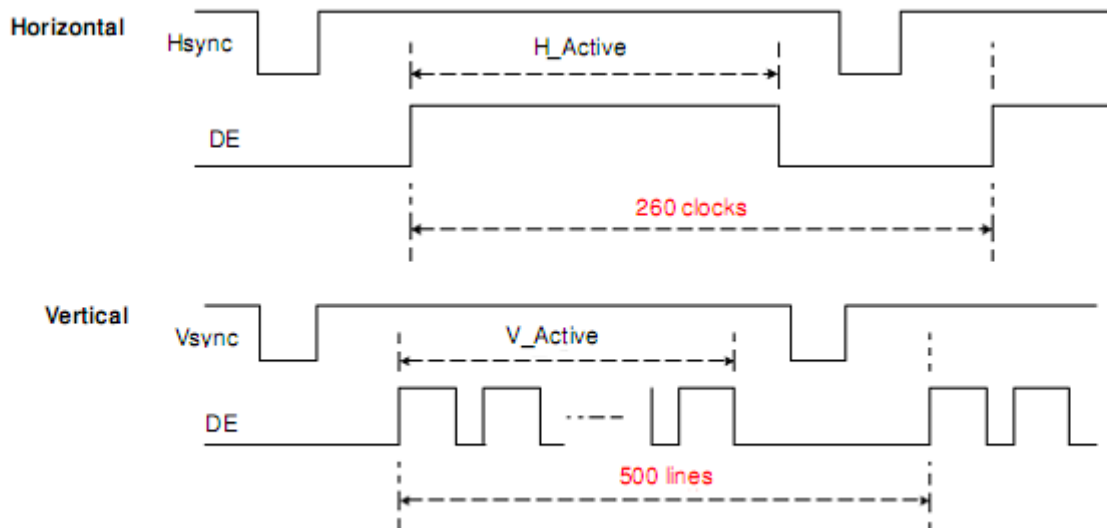
**(21) PLL CONTROL (PLL) (R30H)**

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Controlling PLL	0	0	0	0	1	1	0	0	0	0	30H
	0	1	-	-	-	-	FRS[3:0]			04H	

The command controls the PLL clock frequency. The PLL structure must support the following frame rates:

**FMR[3:0]:** Frame rate setting

FRS	Frame rate	FRS	Frame rate
0000	10Hz	1000	90Hz
0001	20Hz	1001	100Hz
0010	30Hz	1010	110Hz
0011	40Hz	1011	120Hz
0100	50Hz	1100	130Hz
0101	60Hz	1101	140Hz
0110	70Hz	1110	150Hz
0111	80Hz	1111	200Hz





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### (22) TEMPERATURE SENSOR CALIBRATION (TSC) (R40H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Sensing Temperature	0	0	0	1	0	0	0	0	0	0	40H
	1	1	D10/TS7	D9/TS6	D8/TS5	D7/TS4	D6/TS3	D5/TS2	D4/TS1	D3/TS0	00H
	1	1	D2	D1	D0	-	-	-	-	-	00H

This command enables internal or external temperature sensor, and reads the result.

**TS[7:0]:** When TSE (R41h) is set to 0, this command reads internal temperature sensor value.

**D[10:0]:** When TSE (R41h) is set to 1, this command reads external LM75 temperature sensor value.

TS[7:0]/D[10:3]	Temp. (°C)	TS[7:0]/D[10:3]	Temp. (°C)	TS[7:0]/D[10:3]	Temp. (°C)
1110_0111	-25	0000_0000	0	0001_1001	25
1110_1000	-24	0000_0001	1	0001_1010	26
1110_1001	-23	0000_0010	2	0001_1011	27
1110_1010	-22	0000_0011	3	0001_1100	28
1110_1011	-21	0000_0100	4	0001_1101	29
1110_1100	-20	0000_0101	5	0001_1110	30
1110_1101	-19	0000_0110	6	0001_1111	31
1110_1110	-18	0000_0111	7	0010_0000	32

### (23) TEMPERATURE SENSOR ENABLE (TSE) (R41H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Enable Temperature Sensor /Offset	0	0	0	1	0	0	0	0	0	1	41H
	0	1	TSE	-	-	-	TO[3:0]				00H

This command selects Internal or External temperature sensor.

**TSE:** Internal temperature sensor switch

0: Enable (default)

1: Disable; using external sensor.

**TO[3:0]:** Temperature offset.

TO[3:0]	Calibration
0000 b	+0 (Default)
0001	+1
0010	+2
0011	+3
0100	+4
0101	+5
0110	+6
0111	+7

TO[3:0]	Calibration
1000	-8
1001	-7
1010	-6
1011	-5
1100	-4
1101	-3
1110	-2
1111	-1





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**(24) TEMPERATURE SENSOR WRITE (TSW) (R42H)**

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Write External Temperature Sensor	0	0	0	1	0	0	0	0	1	0	42H
	0	1	WATTR[7:0]								00H
	0	1	WMSB[7:0]								00H
	0	1	WLSB[7:0]								00H

This command writes the temperature sensed by the temperature sensor.

**WATTR[7:6]:** I<sup>2</sup>C Write Byte Number

- 00b : 1 byte (head byte only)
- 01b : 2 bytes (head byte + pointer)
- 10b : 3 bytes (head byte + pointer + 1<sup>st</sup> parameter)
- 11b : 4 bytes (head byte + pointer + 1<sup>st</sup> parameter + 2<sup>nd</sup> parameter)

**WATTR[5:3]:** User-defined address bits (A2, A1, A0)

**WATTR[2:0]:** Pointer setting

**WMSB[7:0]:** MSByte of write-data to external temperature sensor

**WLSB[7:0]:** LSByte of write-data to external temperature sensor

**(25) TEMPERATURE SENSOR READ (TSR) (R43H)**

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Read External Temperature Sensor	0	0	0	1	0	0	0	0	1	1	43H
	1	1	RMSB[7:0]								00H
	1	1	RLSB[7:0]								00H

This command reads the temperature sensed by the temperature sensor.

**RMSB[7:0]:** MSByte read data from external temperature sensor

**RLSB[7:0]:** LSByte read data from external temperature sensor

**(26) PANEL GLASS CHECK (PBC)**

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Check Panel Glass	0	0	0	1	0	0	0	1	0	0	44H
	1	1	-	-	-	-	-	-	-	PSTA	00H

This command is used to enable panel check, and to disable after reading result.

**PSTA:0:** Panel check fail (panel broken)

1: Panel check pass



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**(27) VCOM AND DATA INTERVAL SETTING (CDI) (R50H)**

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set Interval between VCOM and Data	0	0	0	1	0	1	0	0	0	0
	0	1	BDZ	-	BDV[1:0]	-	-	DDX[1:0]		
	0	1	-	-	-	-	CDI[3:0]			

50h  
31h  
07H

This command indicates the interval of VCOM and data output. When setting the vertical back porch, the total blanking will be kept (20 Hsync).

**BDZ:** Border Hi-Z control

**0:** Border output Hi-Z disabled (default)

**1:** Border output Hi-Z enabled

**BDV[1:0]:** Border LUT selection

KWR mode (KW/R=0)

DDX[0]	BDV[1:0]	LUT
0	00	LUTBD
	01	LUTR
	10	LUTW
	11	LUTK
1 (Default)	00	LUTK
	01	LUTW
	10	LUTR
	11	LUTBD

KW mode (KW/R=1)

DDX[0]	BDV[1:0]	LUT
0	00	LUTBD
	01	LUTKW (1 → 0)
	10	LUTWK (0 → 1)
	11	LUTKK (0 → 0)
1 (Default)	00	LUTKK (0 → 0)
	01	LUTWK (1 → 0)
	10	LUTKW (0 → 1)
	11	LUTBD



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**DDX[1:0]:** Data polarity.

Under KWR mode (KW/R=0):

DDX[1] is for RED data.  
DDX[0] is for K/W data,

DDX[1:0]	Data (Red, K/W)	LUT
00	00	LUTW
	01	LUTK
	10	LUTR
	11	LUTR
01 (Default)	00	LUTK
	01	LUTW
	10	LUTR
	11	LUTR

DDX[1:0]	Data (Red, K/W)	LUT
10	00	LUTR
	01	LUTR
	10	LUTW
	11	LUTK
11	00	LUTR
	01	LUTR
	10	LUTK
	11	LUTW

Under KW mode (KW/R=1):

DDX[1]=0 is for KW mode with NEW/OLD,  
DDX[1]=1 is for KW mode without NEW/OLD.

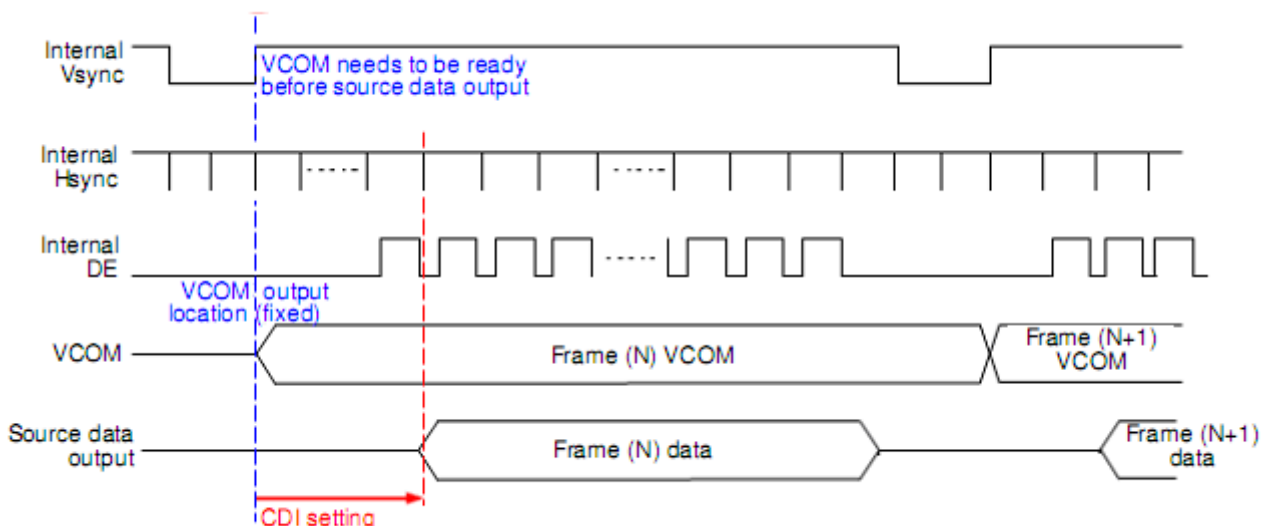
DDX[1:0]	Data (NEW, OLD)	LUT
00	00	LUTWW (0 → 0)
	01	LUTKW (1 → 0)
	10	LUTWK (0 → 1)
	11	LUTKK (1 → 1)
01 (Default)	00	LUTKK (0 → 0)
	01	LUTWK (1 → 0)
	10	LUTKW (0 → 1)
	11	LUTWW (1 → 1)

DDX[1:0]	Data (NEW)	LUT
10	0	LUTKW (1 → 0)
	1	LUTWK (0 → 1)
11	0	LUTWK (1 → 0)
	1	LUTKW (0 → 1)

**CDI[3:0]:** VCOM and data interval

CDI[3:0]	VCOM and Data Interval
0000 b	17 hsync
0001	16
0010	15
0011	14
0100	13
0101	12
0110	11
0111	10 (Default)

CDI[3:0]	VCOM and Data Interval
1000	9
1001	8
1010	7
1011	6
1100	5
1101	4
1110	3
1111	2





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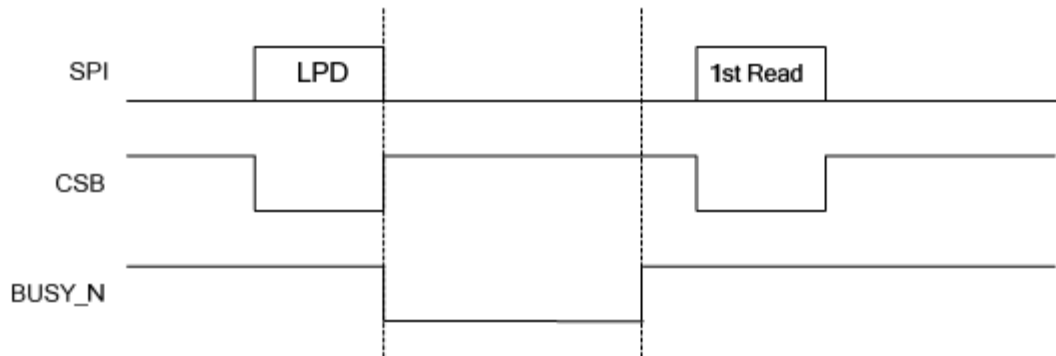
### (28) LOW POWER DETECTION (LPD) (R51H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Detect Low Power	0	0	0	1	0	1	0	0	0	1	51h
	1	1	-	-	-	-	-	-	-	LPD	01h

This command indicates the input power condition. Host can read this flag to learn the battery condition.

**LPD:** Internal Low Power Detection Flag

- 0: Low power input ( $V_{DD} < 2.5V, 2.4V, 2.3V, \text{ or } 2.2V$ , selected by LVD\_SEL[1:0] in command LVSEL)
- 1: Normal status (default)



### (30) TCON SETTING (TCON) (R60H)

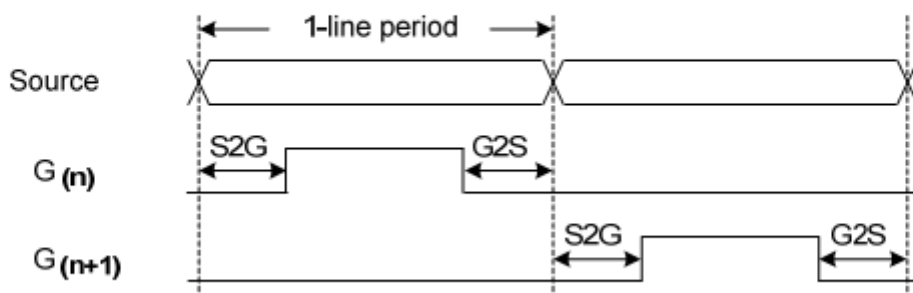
Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Gate/Source Non-overlap Period	0	0	0	1	1	0	0	0	0	0	60h
	0	1	S2G[3:0]				G2S[3:0]				22h

This command defines non-overlap period of Gate and Source.

**S2G[3:0] or G2S[3:0]:** Source to Gate / Gate to Source Non-overlap period

S2G[3:0] or G2S[3:0]	Period	S2G[3:0] or G2S[3:0]	Period
0000 b	4	1000 b	36
0001	8	1001	40
<b>0010</b>	<b>12 (Default)</b>	1010	44
0011	16	1011	48
0100	20	1100	52
0101	24	1101	56
0110	28	1110	60
0111	32	1111	64

Period Unit = 667 nS.





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**(31) RESOLUTION SETTING (TRES) (R61H)**

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Display Resolution	0	0	0	1	1	0	0	0	0	1	61h
	0	1	HRES[7:3]					0	0	0	F0h
	0	1	-	-	-	-	-	-	VRES[9]	VRES[8]	02h
	0	1	VRES[7:0]								00h

This command defines resolution setting.

**HRES[7:3]:** Horizontal Display Resolution (Value range: 01h ~ 1Eh)

**VRES[9:0]:** Vertical Display Resolution (Value range: 01h ~ 200h)

Active channel calculation, assuming HST[7:0]=0, VST[8:0]=0:

Gate: First active gate = G0;  
Last active gate = VRES[9:0] - 1

Source: First active source = S0;  
Last active source = HRES[7:3]\*8 - 1

Example: 128 (source) x 272 (gate), assuming HST[7:0]=0, VST[8:0]=0

Gate: First active gate = G0,  
Last active gate = G271; (VRES[8:0] = 272, 272 - 1 = 271)

Source: First active source = S0,  
Last active source = S127; (HRES[7:3]=16, 16\*8 - 1 = 127)

**(32) GATE/SOURCE START SETTING (GSST) (R65H)**

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Gate/Source Start	0	0	0	1	1	0	0	1	0	1	65h
	0	1	HST[7:3]					0	0	0	00h
	0	1	-	-	-	-	-	-	-	VST[8]	00h
	0	1	VST[7:0]								00h

This command defines resolution start gate/source position.

**HST[7:3]:** Horizontal Display Start Position (Source). (Value range: 00h ~ 1Dh)

**VST[8:0]:** Vertical Display Start Position (Gate). (Value range: 000h ~ 1FFh)

Example : For 128(Source) x 240(Gate)

HST[7:3] = 4 (HST[7:0] = 4\*8 = 32),  
VST[8:0] = 32

Gate: First active gate = G32 (VST[8:0] = 32),  
Last active gate = G271 (VRES[8:0] = 240, VST[8:0] = 32, 240-1+32=271)

Source: First active source = S32 (HST[7:0]= 32),  
Last active source = S239 (HRES[8:0] = 128, HST[7:0] = 32, 128-1+32=239)



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### (35) AUTO MEASURE VCOM (AMV) (R80H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Automatically measure VCOM	0	0	1	0	0	0	0	0	0	0
	0	1	-	-	AMVT[1:0]		XON	AMVS	AMV	AMVE

This command reads the IC status.

**AMVT[1:0]:** Auto Measure VCOM Time

00b: 3s

10b: 8s

01b: 5s (default)

11b: 10s

**XON:** All Gate ON of AMV

0: Gate normally scan during Auto Measure VCOM period. (default)

1: All Gate ON during Auto Measure VCOM period.

**AMVS:** Source output of AMV

0: Source output 0V during Auto Measure VCOM period. (default)

1: Source output VDHR during Auto Measure VCOM period.

**AMV:** Analog signal

0: Get VCOM value with the VV command (R81h) (default)

1: Get VCOM value in analog signal. (External analog to digital converter)

**AMVE:** Auto Measure VCOM Enable (/Disable)

0: No effect (default)

1: Trigger auto VCOM sensing.

### (36) VCOM VALUE (VV) (R81H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Automatically measure VCOM	0	0	1	0	0	0	0	0	0	1
	1	1	-	-	VV[5:0]					

This command gets the VCOM value.

**W[5:0]:** VCOM Value Output

VV [5:0]	VCOM Voltage (V)	VV [5:0]	VCOM Voltage (V)	VV [5:0]	VCOM Voltage (V)
00 0000b	-0.10	01 0100b	-1.10	10 1000b	-2.10
00 0001b	-0.15	01 0101b	-1.15	10 1001b	-2.15
00 0010b	-0.20	01 0110b	-1.20	10 1010b	-2.20
00 0011b	-0.25	01 0111b	-1.25	10 1011b	-2.25
00 0100b	-0.30	01 1000b	-1.30	10 1100b	-2.30
00 0101b	-0.35	01 1001b	-1.35	10 1101b	-2.35
00 0110b	-0.40	01 1010b	-1.40	10 1110b	-2.40
00 0111b	-0.45	01 1011b	-1.45	10 1111b	-2.45
00 1000b	-0.50	01 1100b	-1.50	11 0000b	-2.50
00 1001b	-0.55	01 1101b	-1.55	11 0001b	-2.55
00 1010b	-0.60	01 1110b	-1.60	11 0010b	-2.60
00 1011b	-0.65	01 1111b	-1.65	11 0011b	-2.65
00 1100b	-0.70	10 0000b	-1.70	11 0100b	-2.70
00 1101b	-0.75	10 0001b	-1.75	11 0101b	-2.75
00 1110b	-0.80	10 0010b	-1.80	11 0110b	-2.80
00 1111b	-0.85	10 0011b	-1.85	11 0111b	-2.85
01 0000b	-0.90	10 0100b	-1.90	11 1000b	-2.90
01 0001b	-0.95	10 0101b	-1.95	11 1001b	-2.95
01 0010b	-1.00	10 0110b	-2.00	11 1010b	-3.00
01 0011b	-1.05	10 0111b	-2.05	11 1011b	-3.05



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(37) VCOM\_DC SETTING (VDCS) (R82H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set VCOM_DC	0	0	1	0	0	0	0	0	1	0
	0	1	-	-	VDCS[5:0]					

82h  
00h

This command sets VCOM\_DC value

VDCS[5:0]: VCOM\_DC Setting

VDCS [5:0]	VCOM Voltage (V)	VDCS [5:0]	VCOM Voltage (V)	VDCS [5:0]	VCOM Voltage (V)
00 0000b	-0.10	01 0100b	-1.10	10 1000b	-2.10
00 0001b	-0.15	01 0101b	-1.15	10 1001b	-2.15
00 0010b	-0.20	01 0110b	-1.20	10 1010b	-2.20
00 0011b	-0.25	01 0111b	-1.25	10 1011b	-2.25
00 0100b	-0.30	01 1000b	-1.30	10 1100b	-2.30
00 0101b	-0.35	01 1001b	-1.35	10 1101b	-2.35
00 0110b	-0.40	01 1010b	-1.40	10 1110b	-2.40
00 0111b	-0.45	01 1011b	-1.45	10 1111b	-2.45
00 1000b	-0.50	01 1100b	-1.50	11 0000b	-2.50
00 1001b	-0.55	01 1101b	-1.55	11 0001b	-2.55
00 1010b	-0.60	01 1110b	-1.60	11 0010b	-2.60
00 1011b	-0.65	01 1111b	-1.65	11 0011b	-2.65
00 1100b	-0.70	10 0000b	-1.70	11 0100b	-2.70
00 1101b	-0.75	10 0001b	-1.75	11 0101b	-2.75
00 1110b	-0.80	10 0010b	-1.80	11 0110b	-2.80
00 1111b	-0.85	10 0011b	-1.85	11 0111b	-2.85
01 0000b	-0.90	10 0100b	-1.90	11 1000b	-2.90
01 0001b	-0.95	10 0101b	-1.95	11 1001b	-2.95
01 0010b	-1.00	10 0110b	-2.00	11 1010b	-3.00
01 0011b	-1.05	10 0111b	-2.05	others	-3.00



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**(38) PARTIAL WINDOW (PTL) (R90H)**

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0		
Set Partial Window	0	0	1	0	0	1	0	0	0	0	90h	
	0	1	HRST[7:3]					0	0	0		00h
	0	1	HRED[7:3]					1	1	1		Efh
	0	1	-	-	-	-	-	-	-	VRST[8]	00h	
	0	1	VRST[7:0]									00h
	0	1	-	-	-	-	-	-	-	VRED[8]	01h	
	0	1	VRED[7:0]									FFh
	0	1	-	-	-	-	-	-	-	PT_SCAN	01h	

This command sets partial window.

**HRST[7:3]:** Horizontal start channel bank. (Value range: 00h~1Dh)

**HRED[7:3]:** Horizontal end channel bank. (Value range: 00h~1Dh). HRED must be greater than HRST.

**VRST[8:0]:** Vertical start line. (Value range: 000h~1FFh)

**VRED[8:0]:** Vertical end line. (Value range: 000h~1FFh). VRED must be greater than VRST.

**PT\_SCAN:** 0: Gates scan only inside of the partial window.

1: Gates scan both inside and outside of the partial window. (default)

**(39) PARTIAL IN (PTIN) (R91H)**

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Partial In	0	0	1	0	0	1	0	0	0	1	91h

This command makes the display enter partial mode.

**(40) PARTIAL OUT (PTOUT) (R92H)**

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Partial Out	0	0	1	0	0	1	0	0	1	0	92h

This command makes the display exit partial mode and enter normal mode.

**(42) ACTIVE PROGRAM (APG) (RA1H)**

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Active Program OTP	0	0	1	0	1	0	0	0	0	1	A1h

After this command is transmitted, the programming state machine would be activated.

The BUSY\_N flag would fall to 0 until the programming is completed.





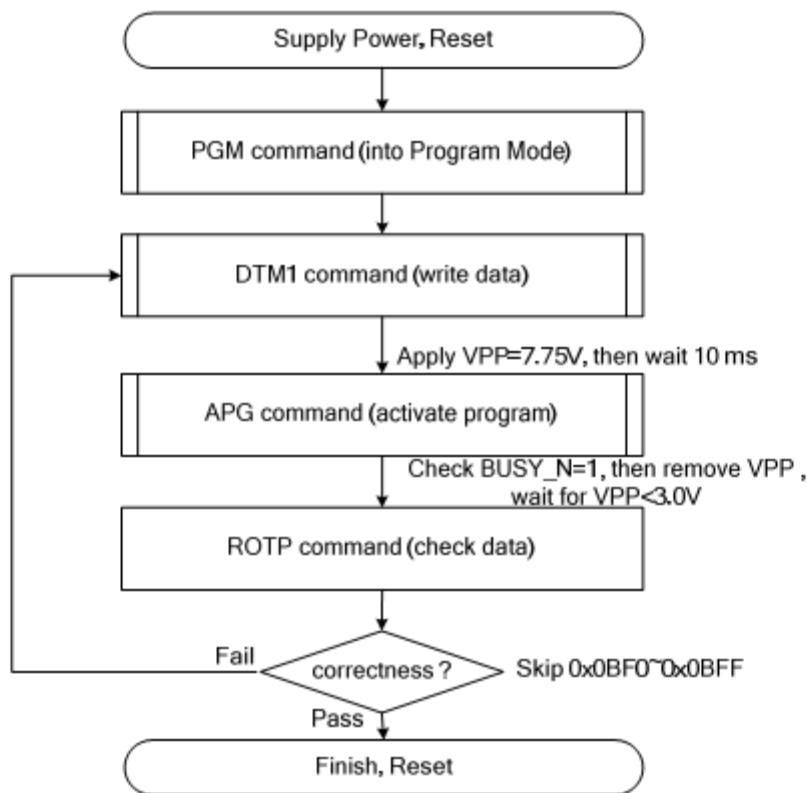
File Name	Specification For HINK 3.7" EPD	Module Number	HINK-E037A39
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**(43) READ OTP DATA (ROTP) (RA2H)**

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	A2h	
Read OTP data for check	0	0	1	0	1	0	0	0	1	0		
	1	1	The data of address 0x000 in the OTP									--
	1	1	The data of address 0x001 in the OTP									--
	1	1	:									--
	1	1	The data of address (n-1) in the OTP									--
	1	1	The data of address (n) in the OTP									--

The command is used for reading the content of OTP for checking the data of programming.

The value of (n) is depending on the amount of programmed data, the max address = 0x17FF.



The sequence of programming OTP.



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**(44) CASCADE SETTING (CCSET) (RE0H)**

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set Cascade Option	0	0	1	1	1	0	0	0	0	0
	0	1	-	-	-	-	-	-	TSFIX	CCEN

This command is used for cascade.

**TSFIX:** Let the value of slave's temperature is same as the master's.

0: Temperature value is defined by internal temperature sensor / external LM75. (default)

1: Temperature value is defined by TS\_SET[7:0] registers.

**CCEN:** Output clock enable/disable.

0: Output 0V at CL pin. (default)

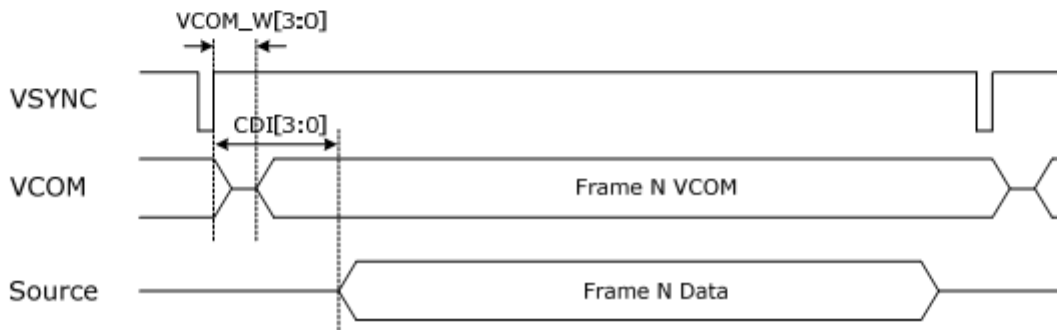
1: Output clock at CL pin to slave chip.

**(45) POWER SAVING (PWS) (RE3H)**

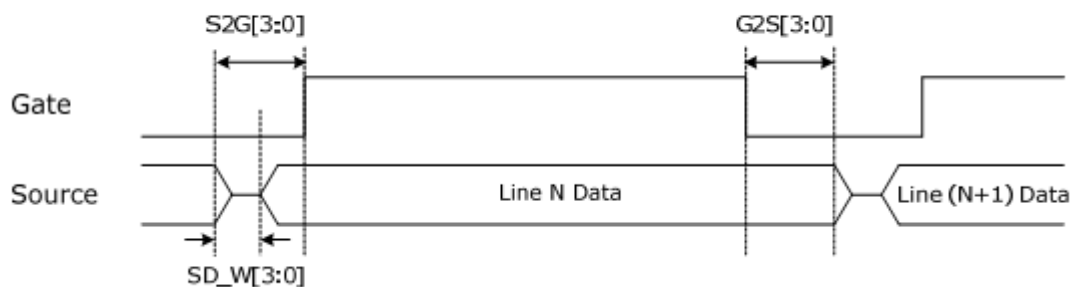
Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Power Saving for VCOM & Source	0	0	1	1	1	0	0	0	1	1
	0	1	VCOM_W[3:0]				SD_W[3:0]			

This command is set for saving power during refreshing period. If the output voltage of VCOM / Source is from negative to positive or from positive to negative, the power saving mechanism will be activated. The active period width is defined by the following two parameters.

**VCOM\_W[3:0]:** VCOM power saving width (Unit: line period)



**SD\_W[3:0]:** Source power saving width (Unit: 660nS)





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**(46) LVD VOLTAGE SELECT (LVSEL) (RE4H)**

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Select LVD Voltage	0	0	1	1	1	0	0	1	0	0	E4h
	0	1	-	-	-	-	-	-	LVD_SEL[1:0]		03h

LVD\_SEL[1:0]: Low Power Voltage selection

LVD_SEL[1:0]	LVD value
00	< 2.2 V
01	< 2.3 V
10	< 2.4 V
11	< 2.5 V (default)

**(47) FORCE TEMPERATURE (TSSET) (RE5H)**

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Force Temperature Value for Cascade	0	0	1	1	1	0	0	1	0	1	E5h
	0	1	TS_SET[7:0]								00h

This command is used for cascade to fix the temperature value of master and slave chip.



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### 11. Reference Circuit

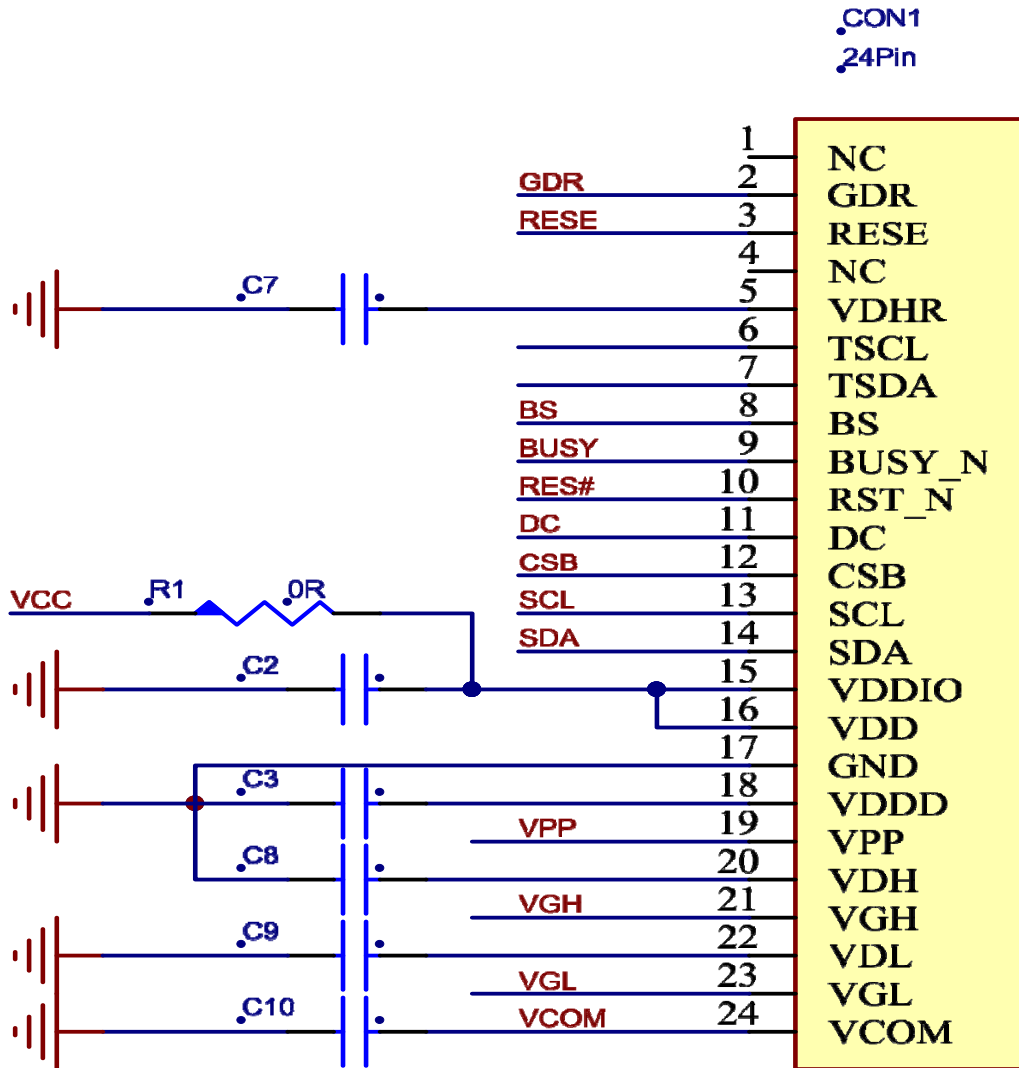
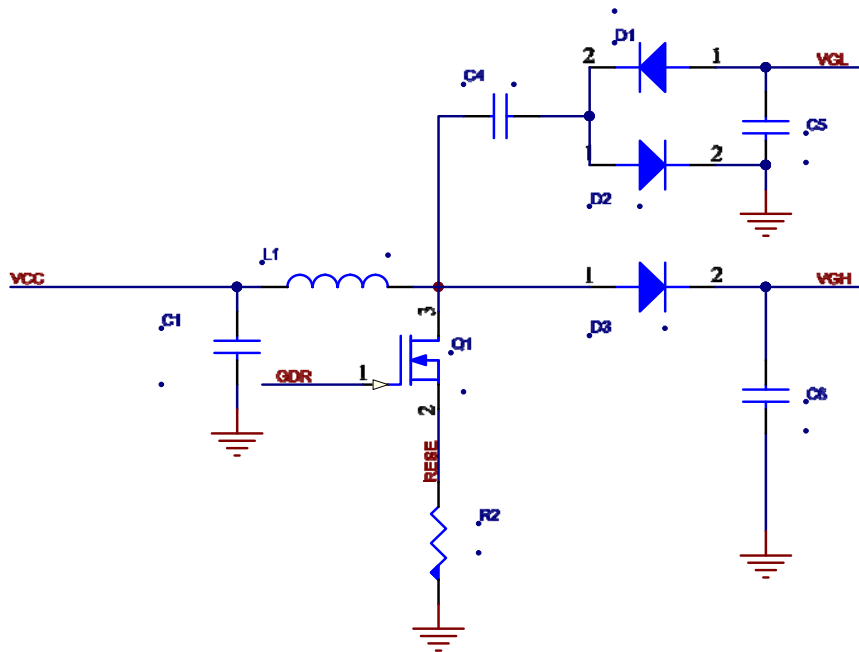


Figure. 11-1



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Part Name	UC8253 Value /quirement/Reference Part
C1—C3	1uF/0603;X5R/X7R;Voltage Rating: 25V
C4	4.7uF/0603;X5R/X7R;Voltage Rating: 25V
C5-C10	1uF/0603;X5R/X7R;Voltage Rating: 25V
D1—D3	MBR0530 1) Reverse DC voltage $\geq 30V$ 2) Forward current $\geq 500mA$ 3) Forward voltage $\leq 430mV$
R2	0.47 $\Omega$ /0603: 1% variation
Q1	NMOS:Si1308EDL 1) Drain-Source breakdown voltage $\geq 30V$ 2) $V_{gs(th)} = 0.9 (Typ) , 1.3V (Max)$ 3) $R_{ds(on)} \leq 2.1 \Omega @ V_{gs}=2.5V$
L1	10uH/Taiyo Yuden NR4018T100M DCR < 0.5 ohm, Isat $\geq 1.2A @ 25^\circ C$



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## 12. ABSOLUTE MAXIMUM RATING

Table 12-1: Maximum Ratings

Symbol	Parameter	Rating	Unit	Humidity	Unit	Note
V <sub>DD</sub>	Logic supply voltage	-0.5 to +6.0	V	-	-	
T <sub>OPR</sub>	Operation temperature range	0 to 40	°C	45 to70	%	Note12-1
T <sub>ttg</sub>	Transportation temperature range	-25 to 60	°C	-	-	Note12-2
T <sub>stg</sub>	Storage condition	0 to 40	°C	45 to70	%	Maximum storage time: 5 years
-	After opening the package	0 to 40	°C	45 to70	%	

Note 12-1: We guarantee the single pixel display quality for 0-35°C, but we only guarantee the barcode readable for 35-40°C. Normal use is recommended to refresh every 24 hours.

Note12-2: T<sub>ttg</sub> is the transportation condition, the transport time is within 10 days for -25°C~0°C or 40°C~60°C.

Note 12-3: When the three-color product is stored. The display screen should be kept white and face up. In addition, please be sure to refresh the e-paper every three months.

## 13.DC CHARACTERISTICS

The following specifications apply for: VSS=0V, VCI=3.3V, T<sub>OPR</sub>=25°C.

Table 12-1: DC Characteristics

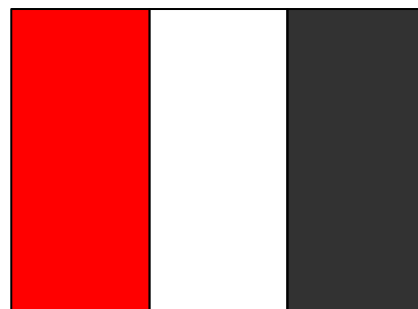
Symbol	Parameter	Test Condition	Applicable pin	Min.	Typ.	Max.	Unit
VDD	VDD operation voltage		VDD	2.5	3.3	3.7	V
VIH	High level input voltage		SDA, SCL, CS#, D/C#, RES#, BS1	0.7VDDIO		VDDIO	V
VIL	Low level input voltage			0		0.3VDDIO	V
VOH	High level output voltage	IOH = 400uA	BUSY	VDDIO-0.4			V
VOL	Low level output voltage	IOL = -400uA		0		0.4	V
I <sub>update</sub>	Module operating current			-	9	-	mA
I <sub>sleep</sub>	Deep sleep mode	VCI=3.3V		-	-	3	uA

The Typical power consumption is measured using associated 25°C waveform with following pattern transition: from horizontal scan pattern to vertical scan pattern. (Note 13-1)

- The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by XingTai.
- Vcom value will be OTP before in factory or present on the label sticker.

Note 13-1

The Typical power consumption





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## 14. AC Characteristics

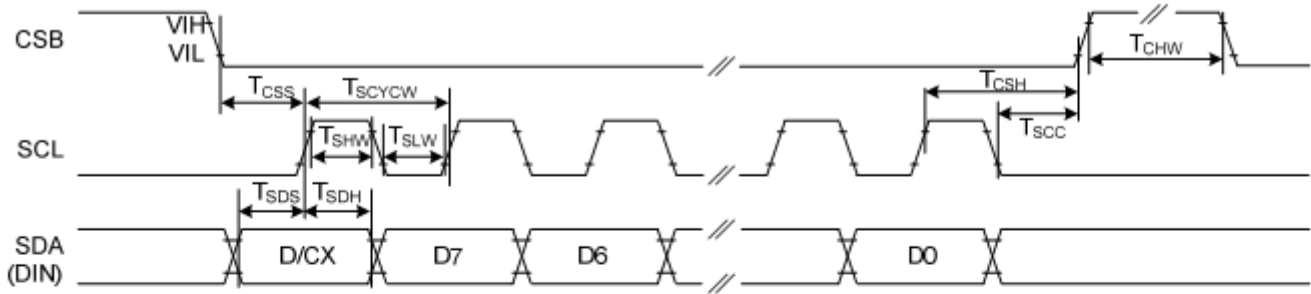


Figure: 3-wire Serial Interface Characteristics (Write mode)

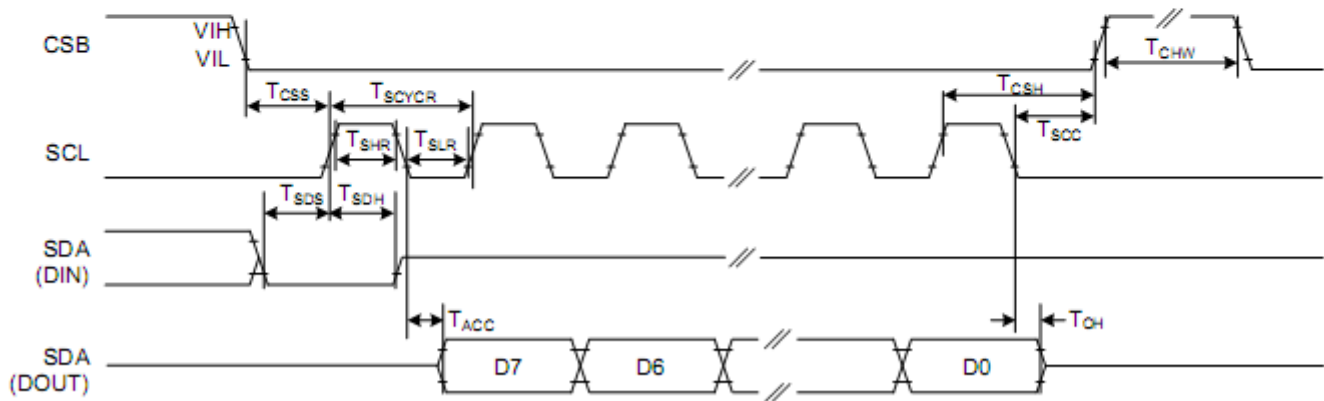


Figure: 3-wire Serial Interface Characteristics (Read mode)

Symbol	Signal / Parameter	Conditions	Min.	Typ.	Max.	Unit
$T_{CSS}$	CSB	Chip select setup time	60			ns
$T_{CSH}$		Chip select hold time	65			ns
$T_{SCC}$		Chip select setup time	20			ns
$T_{CHW}$		Chip select setup time	40			ns
$T_{SCYCW}$	SCL	Serial clock cycle (Write)	100			ns
$T_{SHW}$		SCL "H" pulse width (Write)	35			ns
$T_{SLW}$		SCL "L" pulse width (Write)	35			ns
$T_{SCYCR}$		Serial clock cycle (Read)	350			ns
$T_{SHR}$	SCL	SCL "H" pulse width (Read)	175			ns
$T_{SLR}$		SCL "L" pulse width (Read)	175			ns
$T_{SDS}$	SDA (DIN)	Data setup time	30			ns
$T_{SDH}$		Data hold time	30			ns
$T_{ACC}$	SDA (DOUT)	Access time			350	ns
$T_{OH}$	SDA (DOUT)	Output disable time	15			ns



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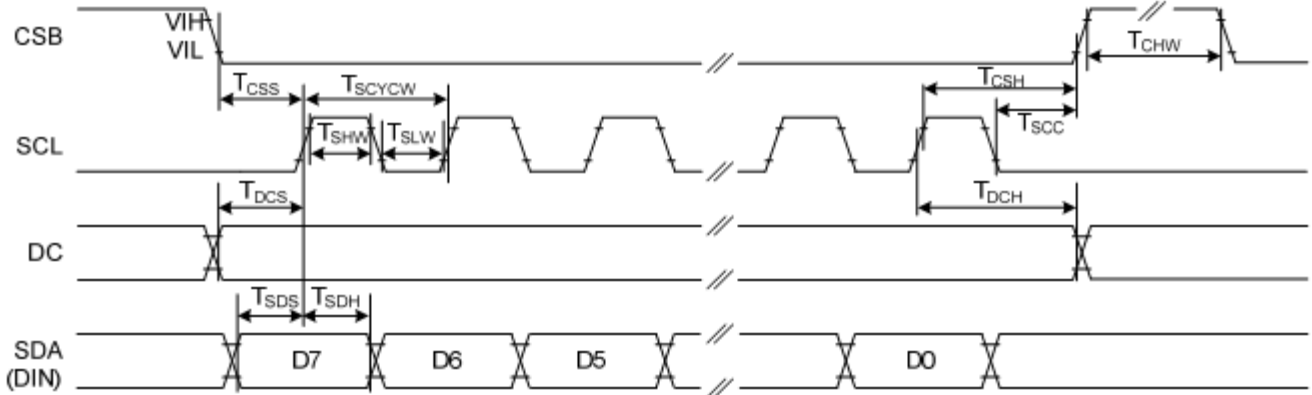


Figure: 4-wire Serial Interface Characteristics (Write mode)

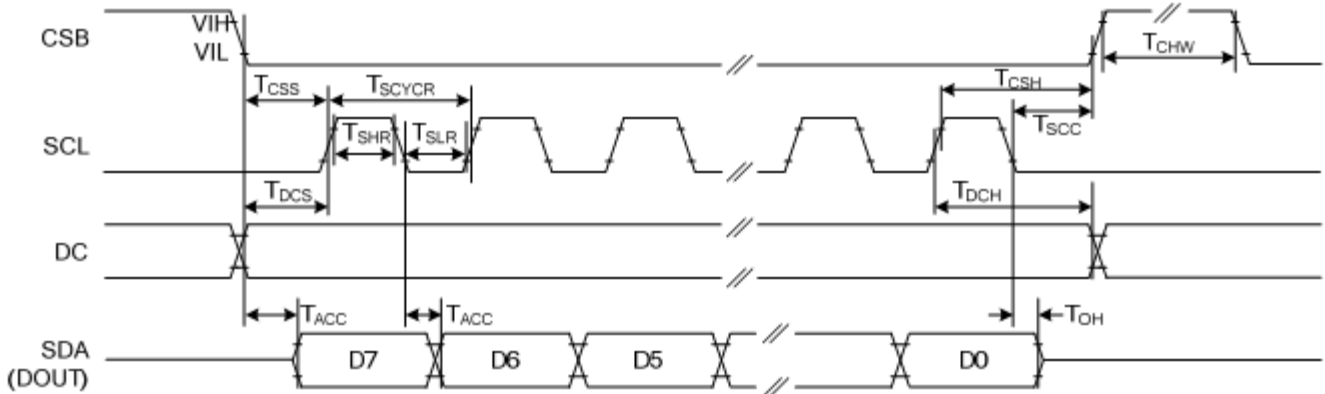


Figure: 4-wire Serial Interface Characteristics (Read mode)

Symbol	Signal / Parameter	Conditions	Min.	Typ.	Max.	Unit
$T_{CSS}$	CSB	Chip select setup time	60			ns
$T_{CSH}$		Chip select hold time	65			ns
$T_{SCC}$		Chip select setup time	20			ns
$T_{CHW}$		Chip select setup time	40			ns
$T_{SCYCW}$	SCL	Serial clock cycle (Write)	100			ns
$T_{SHW}$		SCL "H" pulse width (Write)	35			ns
$T_{SLW}$		SCL "L" pulse width (Write)	35			ns
$T_{SCYCR}$		Serial clock cycle (Read)	350			ns
$T_{SHR}$	SCL	SCL "H" pulse width (Read)	175			ns
$T_{SLR}$		SCL "L" pulse width (Read)	175			ns
$T_{DCS}$	DC	DC setup time	30			ns
$T_{DCH}$		DC hold time	30			ns
$T_{SDS}$	SDA	Data setup time	30			ns
$T_{SDH}$	(DIN)	Data hold time	30			ns
$T_{ACC}$	SDA	Access time			350	ns
$T_{OH}$	(DOUT)	Output disable time	15			ns





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### 15. Power Consumption

Parameter	Symbol	Conditions	TYP	Max	Unit	Remark
Panel power consumption during update	-	25°C	-	180	mAs	-
Deep sleep mode	-	25°C	-	3	uA	-

MAS=update average current ×update time



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## 16. Optical characteristics

### 16.1 Specifications

Measurements are made with that the illumination is under an angle of 45 degrees, the detection is perpendicular unless otherwise specified.

T=25°C

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT	Note
R	Reflectance	White	30	35	-	%	Note 16-1
Gn	2Grey Level	-	-	$KS+(WS-KS) \times n(m-1)$	-	L*	-
CR	Contrast Ratio	-	10	15	-		-
BS	Black State L* value		-	11	14		Note 16-1
	Black State a* value		-		4		Note 16-1
WS	White State L* value		64	65	-		Note 16-1
RS	Red State L* value	Red	25	26.5	29		Note 16-1
	Red State a* value	Red	38	40	44		Note 16-1
Panel	Image Update	Storage and transportation	-	Update the white screen	-	-	-
	Update Time	Operation	-	Suggest Updated once a day	-	-	-

WS : White state, KS : Black state, RS: Red state

Note 16-1 : Luminance meter : i - One Pro Spectrophotometer

Note 16-2: We don't guarantee 5 years pixels display quality for humidity below 45%RH or above 70%RH;

Suggest Updated once a day;

Note 16-3: To increase the black and white screen clear screen when red has refreshed for a long time, the effect is better

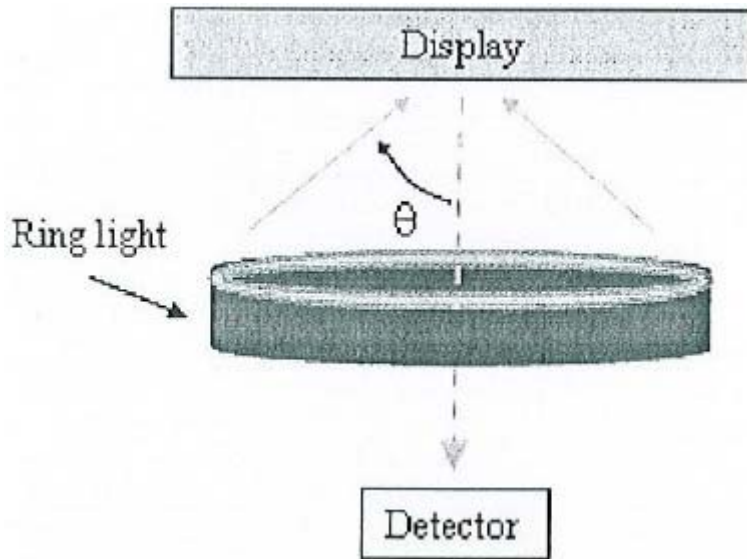


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### 16.2 Definition of contrast ratio

The contrast ratio (CR) is the ratio between the reflectance in a full white area (R1) and the reflectance in a dark area (Rd):

R1: white reflectance      Rd: dark reflectance  
CR = R1/Rd

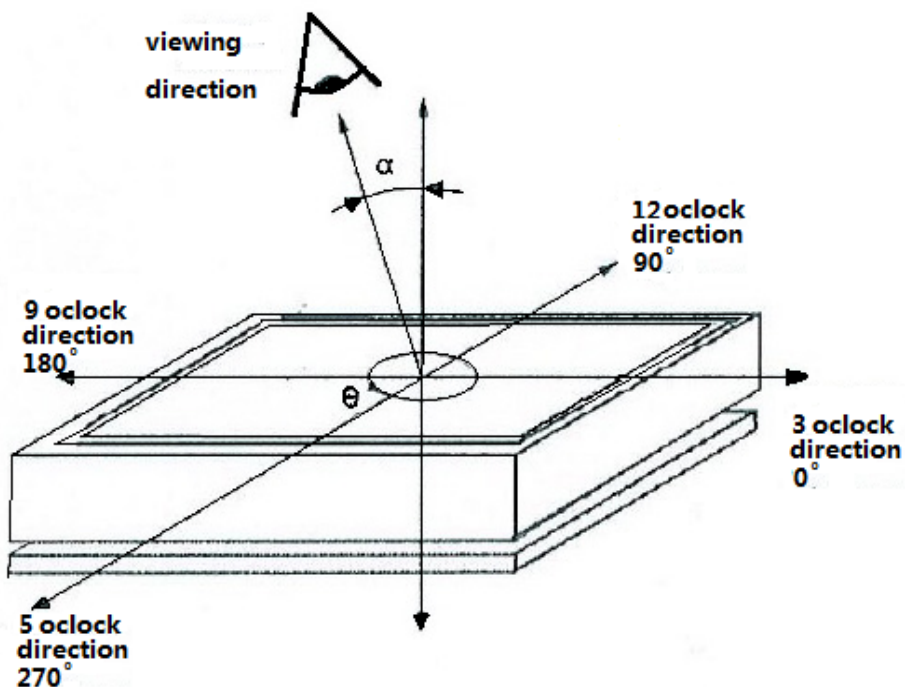


### 16.3 Reflection Ratio

The reflection ratio is expressed as:

$$R = \text{Reflectance Factor}_{\text{white board}} \times (L_{\text{center}} / L_{\text{white board}})$$

$L_{\text{center}}$  is the luminance measured at center in a white area ( $R=G=B=1$ ).  $L_{\text{white board}}$  is the luminance of a standard white board. Both are measured with equivalent illumination source. The viewing angle shall be no more than 2 degrees.





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## 17. HANDLING, SAFETY AND ENVIROMENTAL REQUIREMENTS

### WARNING

The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

### CAUTION

The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.

Disassembling the display module can cause permanent damage and invalidate the warranty agreements.

IPA solvent can only be applied on active area and the back of a glass. For the rest part, it is not allowed.

Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged . Moreover the display is sensitive to static electricity and other rough environmental conditions.

### Mounting Precautions

(1) It's recommended that you consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the module.

(2) It's recommended that you attach a transparent protective plate to the surface in order to protect the EPD. Transparent protective plate should have sufficient strength in order to resist external force.

(3) You should adopt radiation structure to satisfy the temperature specification.

(4) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the PS at high temperature and the latter causes circuit break by electro-chemical reaction.

(5) Do not touch, push or rub the exposed PS with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment. Do not touch the surface of PS for bare hand or greasy cloth. (Some cosmetics deteriorate the PS)

(6) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach the PS. Do not use acetone, toluene and alcohol because they cause chemical damage to the PS.

(7) Wipe off saliva or water drops as soon as possible. Their long time contact with PS causes deformations and color fading.

Product specification	The data sheet contains final product specifications.
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### Limiting values

Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

### Application information

Where application information is given, it is advisory and does not form part of the specification.

### Product Environmental certification

ROHS

### REMARK

All The specifications listed in this document are guaranteed for module only. Post-assembled operation or component(s) may impact module performance or cause unexpected effect or damage and therefore listed specifications is not warranted after any Post-assembled operation.



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## 18. Reliability test

	TEST	CONDITION	METHOD	REMARK
1	High-Temperature Operation	T=40°C, RH=35%RH, For 240Hr		
2	Low-Temperature Operation	T = 0°C for 240 hrs		
3	High-Temperature Storage	T=50°C RH=35%RH For 240Hr Test in white pattern		
4	Low-Temperature Storage	T = -25°C for 240 hrs Test in white pattern		
5	High Temperature, High-Humidity Operation	T=40°C, RH=90%RH, For 168Hr		
6	High Temperature, High-Humidity Storage	T=50°C, RH=90%RH, For 240Hr Test in white pattern		
7	Temperature Cycle	-25°C(30min)~60°C(30min) , 50 Cycle Test in white pattern		
8	Package Vibration	1.04G,Frequency : 10~500Hz Direction : X,Y,Z Duration:1hours in each direction	Full packed for shipment	
9	Package Drop Impact	Drop from height of 100 cm on Concrete surface Drop sequence:1 corner, 3edges, 6face One drop for each.	Full packed for shipment	
10	UV exposure Resistance	765 W/m <sup>2</sup> for 168hrs,40°C		
11	Electrostatic discharge	Machine model: +/-250V,0Ω,200pF		

Actual EMC level to be measured on customer application.

Note1: Stay white pattern for storage and non-operation test.

Note2: Operation is black/white/red pattern , hold time is 150S.

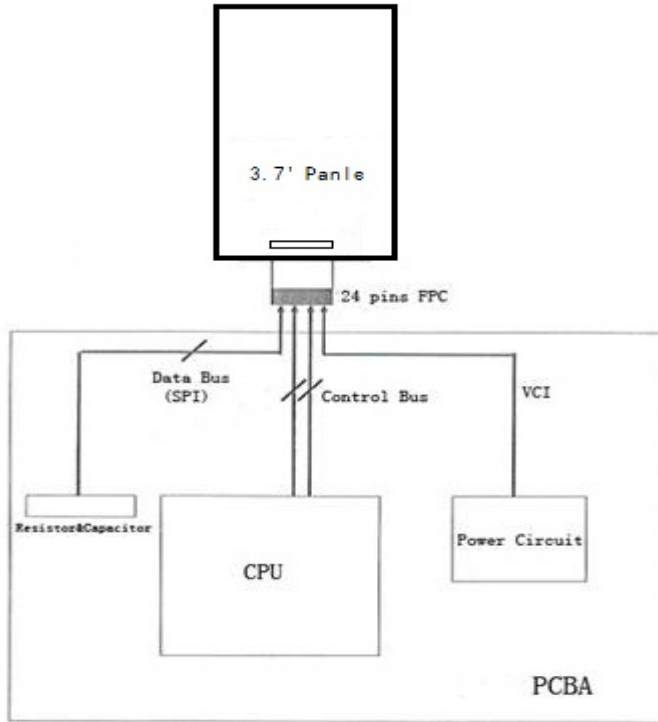
Note3: The function,appearance,opticals should meet the requirements of the test before and after the test.

Note4: Keep testing after 2 hours placing at 20°C-25°C.

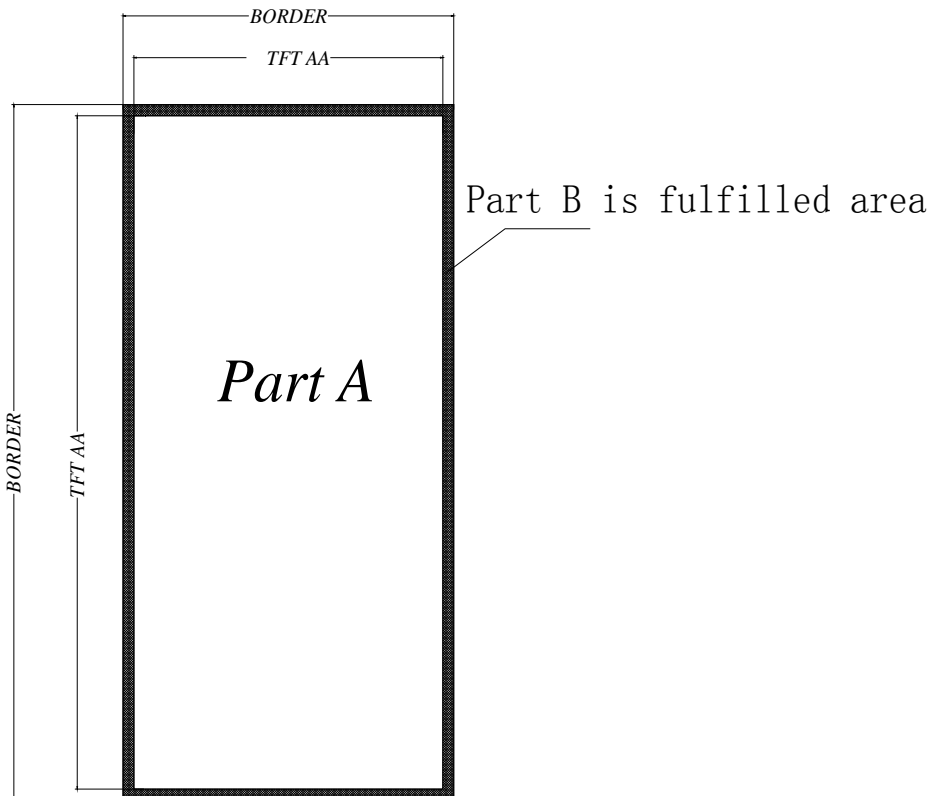


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### 19. Block Diagram



### 20. PartA/PartB specification





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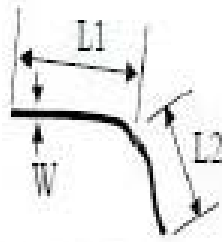
## 21. Point and line standard

Shipment Inspection Standard						
Equipment: Electrical test fixture, Point gauge						
Outline dimension	53(H) × 92.99(V) × 1.05(D)	Unit: mm	Part-A	Active area	Part-B	Border area
Environment	Temperature	Humidity	Illuminance	Distance	Time	Angle
	19°C~25°C	55%±5%RH	800~1300Lux	300 mm	35Sec	
Defet type	Inspection method	Standard		Part-A	Part-B	
Spot	Electric Display	D≤0.25 mm		Ignore	Ignore	
		0.25 mm < D ≤ 0.4 mm		N≤4	Ignore	
		D > 0.4 mm		Not Allow	Ignore	
Display unwork	Electric Display	Not Allow		Not Allow	Ignore	
Display error	Electric Display	Not Allow		Not Allow	Ignore	
Scratch or line defect(include dirt)	Visual/Film card	L≤2 mm, W≤0.2 mm		Ignore	Ignore	
		2.0mm < L ≤ 5.0mm, 0.2 < W ≤ 0.3mm,		N≤2	Ignore	
		L > 5 mm, W > 0.3 mm		Not Allow	Ignore	
PS Bubble	Visual/Film card	D≤0.2mm		Ignore	Ignore	
		0.2mm ≤ D ≤ 0.35mm & N≤4		N≤4	Ignore	
		D > 0.35 mm		Not Allow	Ignore	
Side Fragment	Visual/Film card	X≤6mm, Y≤0.4mm, Do not affect the electrode circuit (Edge chipping)				
		X≤1mm, Y≤1mm, Do not affect the electrode circuit( (Corner chipping) Ignore				
Remark	1.Cannot be defect & failure cause by appearance defect;					
	2.Cannot be larger size cause by appearance defect;					
	L=long W=wide D=point size N=Defects NO					



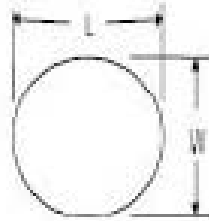


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$$L = L1 + L2$$

Line Defect



$$D = (L + W) / 2$$

Spot Defect

L=long W=wide D=point size



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## 22. Barcode

### 22-1 label appearance



ABBBBBBBCC  
DDDEEEFGGG

### 22-2 QR scanned information (Total 28 code number+ 2 blank spaces)

A BBBBBBBB CC □ DDD EEE F GGG □ H III J KKK  
 ① ② ③ ④ ⑤ ⑥ ⑦ ⑧ ⑨ ⑩ ⑪

- ① A——The factory code
- ② BBBBBBBB——Module name of EPD
- ③ CC——FPL model name
- ④ DDD——Date of production
- ⑤ EEE——Production lot
- ⑥ F——Separator
- ⑦ GGG——FPL Lot
- ⑧ H——Normal Lot
- ⑨ III——TFT、PS、EC.
- ⑩ J——IC
- ⑪ KKK——Serial NO.



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### 23. Packing

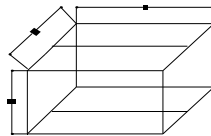
# Packing Spec

Sheet No:

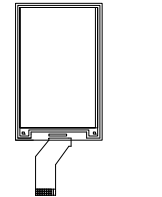
	Part No	HINK-E037A04	DATE	2019. 11. 29	VER	A0	Page	2-1
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一, Package Type: Box

Box No	HINK-E037A03-ZX-A0
Box size	515*322*170
Containment	144 PCS



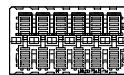
PRODUCT DRAWING



二, Inside package type: Plastic

Tray unit: mm

Plastic Tray	465*280*15	13 pcs
Anti-static foil bags	700*530*0.1	1 pcs
EPE (inside)	408.17*114.75*2	12 pcs
EPE (Up-Down)	485*145*10	2 pcs
EPE (Left-Right)	285*480*10	2 pcs
EPE (Front-back)	310*145*10	2 pcs
Chip board	500*306*5	2 pcs
Quantity/tray	12 pcs	
Tray number/sheet	12+1 Sheets	
Box	1	



Empty tray

Anti-static EPE

Step 1:

Material: Tray, EPE  
Put the product in to the tray and keep the display side up. Then put anti-static EPE in to each holes.

Step 2,

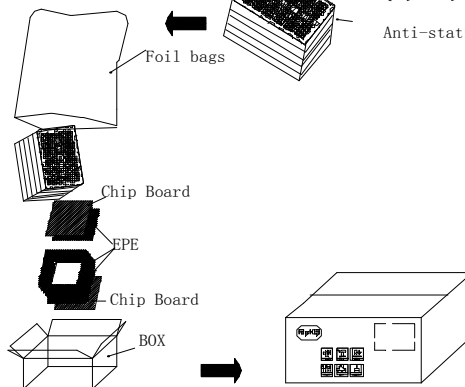
1), Must keep the angle 180 degree placed between the neighboring Plastic trays.  
2), There are 12 layers product, total 4\*12=48 pcs.  
3), An empty Plastic tray intersects put on the top of the plastic trays.

Step 5,

1), Seal the box with adhesive tapes .  
2), Paste the lable onto the exterior box, and the lable can't cover the safety , transfer and RoSH sign.

Step 3,

1), In each case, put 2 bags of desiccant, then seal the trays with adhesive tapes.  
2), Put the trays into foil bags.  
3), heat seal the foil bags.



Step 4,

1), First put a chip board on the bottom of the box, then placed the down EPE, the left - right and front -back EPE.  
2), Placed the sealed products into the box.  
3), The last placed the up EPE on the top of the trays, and place a chip board on it.

Design	C. X. Y	Approve	X. B	Confirm	H.Z.P
Date	2019. 11. 29	Date	2019. 11. 29	Date	2019. 11. 29



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# Packing Spec

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The label outside the carton print as below

90.00	
Label	
Customer Part No	
Customers Item No	A
MFG order No	B
MFG batch No	C
QTY	D
G. W	E
N. W	F
MFG Date	J
Carton No	
Remark	

NOTE:

- "A" Print customer Item No
- "B" Print customer Order No
- "C" Print MFG Batch No (Separate packing for different batch products. Mixed packing available for the odd number of different batch print all the batch NO&QTY accordingly if happened.)
- "D" Print product qty
- "E" Print the G. W
- "F" Print the N. W
- "J" Print the MFG date
- Before packing make sure the FPL batch, item and qty are the same as which on the Final passed card.

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