Specification For HINK 2.7''EPD

Model NO.: HINK-E027A30

Product VER:A0

Customer Approval

Customer	
Approval By	
Date Of Approval	

It will be agreed by the receiver,if not sign back the Specification within 15days.

Prepared By	Checked By	Approval By
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Version	Content	Date	Producer
A0	New release	2021/10/22	Daisy Zhu

CONTENTS

1.General Description

HINK-E027A30 is an Active Matrix Electrophoretic Display (AMEPD), with interface and a reference system design. The 2.7" active area contains 200×300 pixels, and has 1-bit B/W full display capabilities. An integrated circuit contains gate buffer, source buffer, interface, timing control logic, oscillator, DC-DC, SRAM, LUT, VCOM and border are supplied with each panel.

2. Features

- 200×300 pixels display
- High contrast
- High reflectance
- Ultra wide viewing angle
- Ultra low power consumption
- Pure reflective mode
- Bi-stable display
- Commercial temperature range
- Landscape, portrait modes
- Hard-coat antiglare display surface
- Ultra Low current deep sleep mode
- On chip display RAM
- Low voltage detect for supply voltage
- High voltage ready detect for driving voltage
- Internal temperature sensor
- 10-byte OTP space for module identification
- Waveform stored in On-chip OTP
- Serial peripheral interface available
- On-chip oscillator
- On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage
- I2C signal master interface to read external temperature sensor/ built-in temperature sensor

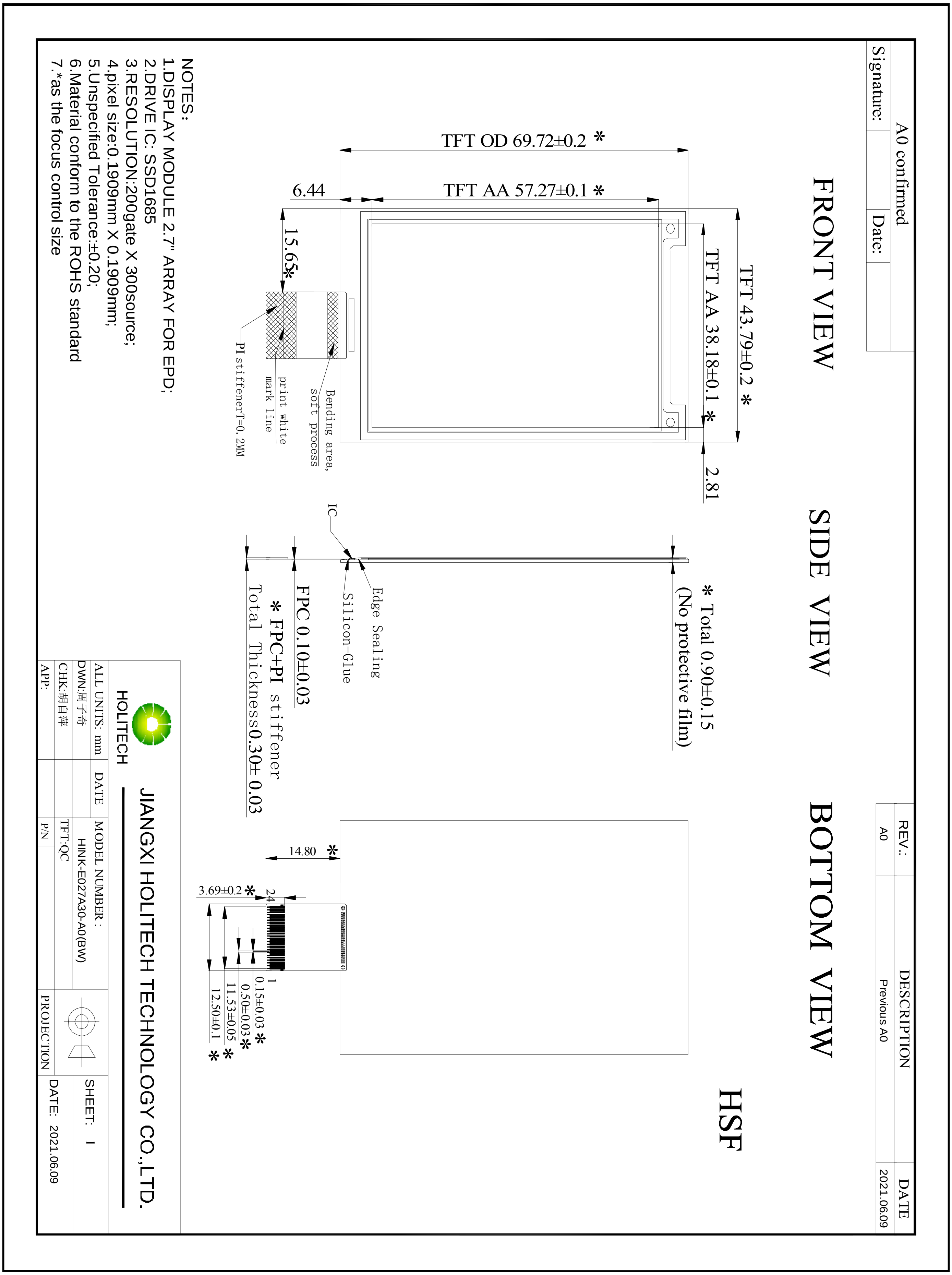
3.Application

Electronic Shelf Label System

4.Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	2.7	Inch	
Display Resolution	200(H)×300(V)	Pixel	Dpi:133
Active Area	38.18(H)×57.27(V)	mm	
Pixel Pitch	0.1909×0.1909	mm	
Pixel Configuration	Rectangle		
Outline Dimension	43.79(H)×69.72(V)×0.9(D)	mm	**Without masking film**
Weight	3±0.5	g	

5. Mechanical Drawing of EPD module



6.Input/Output Terminals

Pin #	Single	Description	Remark
1	NC	No connection and do not connect with other NC pins	Keep Open
2	GDR	N-Channel MOSFET Gate Drive Control	
3	RESE	Current Sense Input for the Control Loop	
4	NC	No connection and do not connect with other NC pins	Keep Open
5	VSH2	Positive Source driving voltage	
6	TSCL	I²C Interface to digital temperature sensor Clock pin	
7	TSDA	I²C Interface to digital temperature sensor Data pin.	
8	BS1	Bus selection pin	Note 6-5
9	BUSY	Busy state output pin	Note 6-4
10	RES #	Reset signal input.	Note 6-3
11	D/C #	Data /Command control pin	Note 6-2
12	CS #	The chip select input connecting to the MCU.	Note 6-1
13	SCL	Serial clock pin for interface.	
14	SDA	Serial data pin for interface.	
15	VDDIO	Power input pin for the Interface.	
16	VCI	Power Supply pin for the chip	
17	VSS	Ground (Digital)	
18	VDD	Core logic power pin	
19	VPP	Power Supply for OTP Programming	
20	VSH1	Positive Source driving voltage	
21	VGH	Power Supply pin for Positive Gate driving voltage and VSH	
22	VSL	Negative Source driving voltage	
23	VGL	Power Supply pin for Negative Gate driving voltage, VCOM and VSL	
24	VCOM	VCOM driving voltage	

Note 6-1: This pin (CS#) is the chip select input connecting to the MCU. The chip is enabled for MCU communication: only when CS# is pulled LOW.

Note 6-2: This pin (D/C#) is Data/Command control pin connecting to the MCU. When the pin is pulled HIGH, the data will be interpreted as data. When the pin is pulled LOW, the data will be interpreted as command.

Note 6-3: This pin (RES#) is reset signal input. The Reset is active low.

Note 6-4: This pin (BUSY) is Busy state output pin. When Busy is High ,the operation of chip should not be interrupted and any commands should not be issued to the module. The driver IC will put Busy pin High when the driver IC is working such as:

- Outputting display waveform;
- Communicating with digital temperature sensor

Note 6-5: This pin (BS1) is for 3-line SPI or 4-line SPI selection. When it is “Low”, 4-line SPI is selected. When it is “High”, 3-line SPI (9 bits SPI) is selected.

7.MCU Interface

7.1 MCU interface selection

The HINK-E027A30 can support 3-wire/4-wire serial peripheral interface. In the Module, the MCU interface is pin selectable by BS1 pins shown in table 7-1.

Table 7-1: Interface pin assignment for different MCU interfaces

	Pin name					
MCU Interface	**BS1**	**RES#**	**CS#**	**D/C#**	**SCL**	**SDA**
4-wire serial peripheral interface (SPI)	L	RES#	CS#	D/C#	SCL	SDI
3-wire serial peripheral interface (SPI) – 9 bits SPI	H	RES#	CS#	L	SCL	SDI

Note：
(1) L is connected to VSS H is connected to VDDIO

7.2 MCU Serial Peripheral Interface (4-wire SPI)

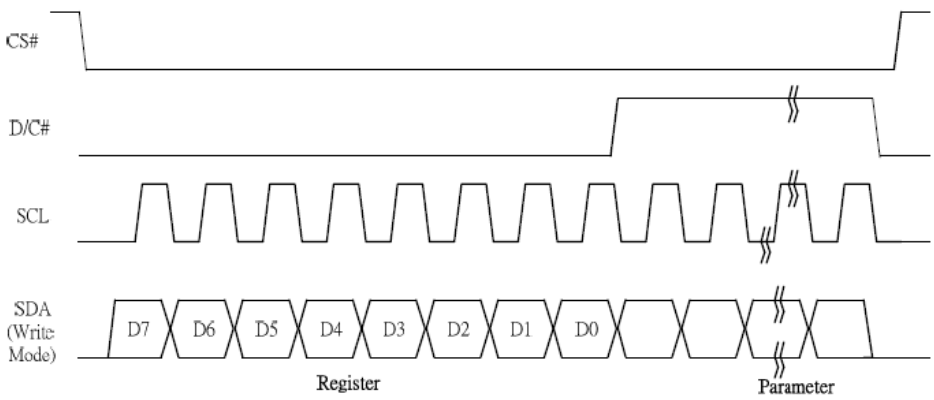
The 4-wire SPI consists of serial clock SCL, serial data SDA, D/C# and CS#. The control pins status in 4-wire SPI in writing command/data is shown in Table 7-2 and the write procedure 4-wire SPI is shown in table 7-2.

Table 7-2 : Control pins status of 4-wire SPI

Function	SCL pin	SDA pin	D/C# pin	CS# pin
Write command	↑	Command bit	L	L
Write data	↑	Data bit	H	L

Note:
(1) L is connected to VSS and H is connected to VDDIO
(2) ↑ stands for rising edge of signal
(3) SDA (Write Mode) is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6, ...D0. The level of D/C# should be kept over the whole byte. The data byte in the shift register is written to the Graphic Display Data RAM (RAM)/Data Byte register or command Byte register according to D/C# pin.

Figure 7-1 Write procedure in 4-wire SPI mode



In the read operation (Command 0x1B, 0x27, 0x2D, 0x2E, 0x2F, 0x35). After CS# is pulled low, the first byte sent is command byte, D/C# is pulled low. After command byte sent, the following byte(s) read are data byte(s), so D/C# bit is then pulled high. An 8-bit data will be shifted out on every clock falling edge. The serial data SDA bit shifting sequence is D7, D6, to D0 bit. Figure7-2 shows the read procedure in 4-wire SPI.

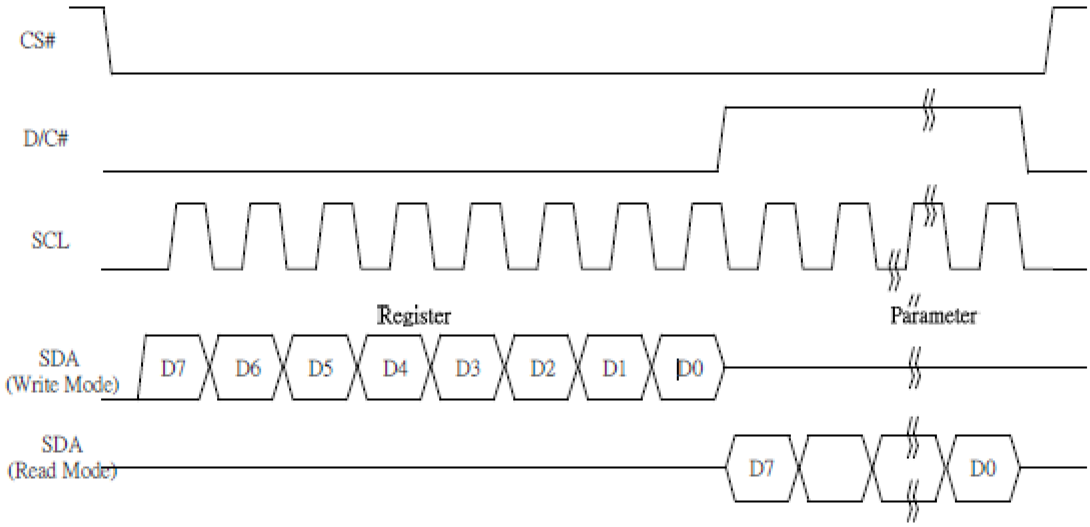


Figure 7-2 Read procedure in 4-wire SPI mode

7.3MCU Serial Peripheral Interface (3-wire SPI)

The 3-wire SPI consists of serial clock SCL, serial data SDA and CS#. The operation is similar to 4-wire SPI while D/C# pin is not used and it must be tied to LOW. The control pins status in 3-wire SPI is shown in Table 7-3.
In the write operation, a 9-bit data will be shifted into the shift register on every clock rising edge. The bit shifting sequence is D/C# bit, D7 bit, D6 bit to D0 bit. The first bit is D/C# bit which determines the following byte is command or data. When D/C# bit is 0, the following byte is command. When D/C# bit is 1, the following byte is data. Table 7-3 shows the write procedure in 3-wire SPI

Table 7-3 : Control pins status of 3-wire SPI

Function	SCL pin	SDI pin	D/C# pin	CS# pin
Write command	↑	Command bit	Tie LOW	L
Write data	↑	Data bit	Tie LOW	L

Note:
(1) L is connected to V_{SS} and H is connected to V_{DDIO}
(2) ↑ stands for rising edge of signal

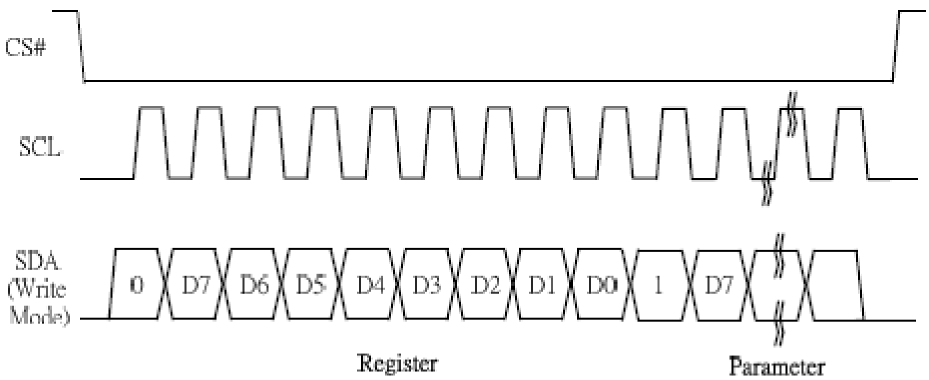


Figure 7-3 Write procedure in 3-wire SPI mode

In the read operation (command 0x1B, 0x27, 0x2D, 0x2E, 0x2F, 0x35). SDA data are transferred in the unit of 9 bits. After CS# pull low, the first byte is command byte, the D/C# bit is as 0 and following with the register byte. After command byte send, the following byte(s) are data byte(s), with D/C# bit is 1. After D/C# bit sending from MCU, an 8-bit data will be shifted out on every clock falling edge. The serial data SDA bit shifting sequence is D7, D6, to D0 bit. Figure 7-4 shows the read procedure in 3-wire SPI.

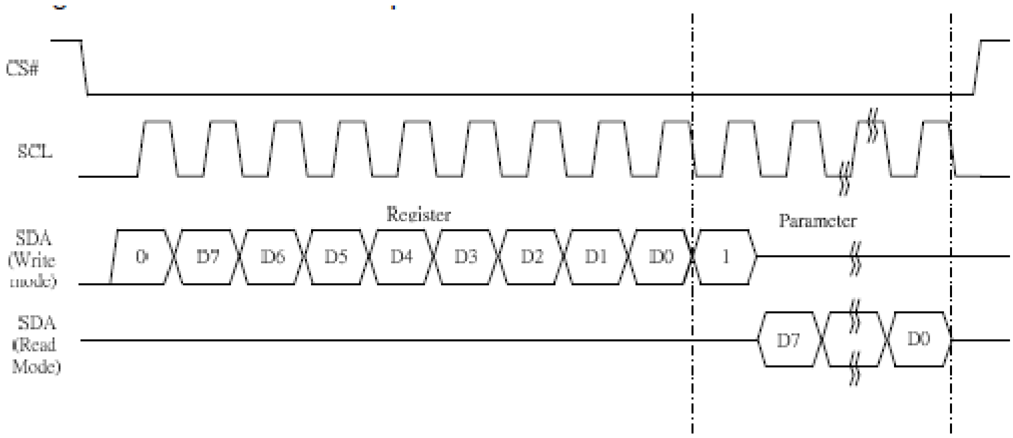


Figure 7-4 Read procedure in 3-wire SPI mode

8. Temperature sensor operation

E027A30 has internal temperature sensor to detect the environment temperature or can communicate with the external temperature sensor by I2C single master interface or can communicate with the external MCU to get the temperature value through SPI. In the SSD1685, there is a dedicated format for the temperature value so that the driver IC can understand it. The format of temperature value is described in following.

The driver IC can communicate with the external temperature sensor through I2C single master interface (TSDA and TSCL). TSDA will be SDA and TSCL will be SCL. TSDA and TSCL are required to connect with external pull-up resistor. Temperature register value of external temperature sensor can be read by command register.

The temperature value is defined by 8-bit binary. The rules are shown as below.

If the Temperature value MSByte bit D11 = 0, then

the temperature is positive and value (DegC) = + (Temperature value)

If the Temperature value MSByte bit D11 = 1, then

the temperature is negative and value (DegC) = **-** (2's complement of Temperature value)

Table 8-1 shows some examples of 8-bit binary temperature value:

8-bit binary (2's complement)	Hexadecimal Value	TR Value [DegC]
0111 1111	7F	12B
0110 0100	64	100
0101 0000	50	80
0100 1011	4B	75
0011 0010	32	50
0001 1001	19	25
0000 0000	00	0
1111 1111	FF	-1
1110 0111	E7	-25
1100 1001	C9	-55

Table 8-1 : Example of 8-bit binary temperature settings for temperature ranges

9.COMMAND TABLE

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	01	0	0	0	0	0	0	0	1	Driver Output control	Gate setting A[8:0]= 17Fh [POR], 384 MUX MUX Gate lines setting as (A[8:0] + 1). B [2:0] = 000 [POR]. Gate scanning sequence and direction B[2]: GD Selects the 1st output Gate GD=0 [POR], G0 is the 1st gate output channel, gate output sequence is G0, G1, G2, G3, … GD=1, G1 is the 1st gate output channel, gate output sequence is G1, G0, G3, G2, … B[1]: SM Change scanning order of gate driver. SM=0 [POR], G0, G1, G2, G3…G382, G383 (left and right gate interlaced) SM=1, G0, G2, G4 …G382, G1, G3, …G383 B[0]: TB TB = 0 [POR], scan from G0 to G383 TB = 1, scan from G383 to G0.
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		0	0	0	0	0	0	0	A_8		
0	1		0	0	0	0	0	B_2	B_1	B_0		
0	0	03	0	0	0	0	0	0	1	1	Gate Driving voltage Control	Set Gate driving voltage A[4:0] = 00h [POR] VGH setting from 10V to 20V
0	1		0	0	0	A_4	A_3	A_2	A_1	A_0		

A[4:0]	VGH	A[4:0]	VGH
00h	20	0Dh	15
03h	10	0Eh	15.5
04h	10.5	0Fh	16
05h	11	10h	16.5
06h	11.5	11h	17
07h	12	12h	17.5
08h	12.5	13h	18
07h	12	14h	18.5
08h	12.5	15h	19
09h	13	16h	19.5
0Ah	13.5	17h	20
0Bh	14	Other	NA
0Ch	14.5		

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	04	0	0	0	0	0	1	0	0	Source Driving voltage Control	Set Source driving voltage A[7:0] = 41h [POR], VSH1 at 15V B [7:0] = A8h [POR], VSH2 at 5V. C[7:0] = 32h [POR], VSL at -15V Remark: VSH1>=VSH2
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		

B[7] = 1,
VSH2 voltage setting from 2.4V to 8.6V

A/B[7:0]	VSH1/VSH2	A/B[7:0]	VSH1/VSH2
8Eh	2.4	AEh	5.6
8Fh	2.5	AFh	5.7
90h	2.6	B0h	5.8
91h	2.7	B1h	5.9
92h	2.8	B2h	6
93h	2.9	B3h	6.1
94h	3	B4h	6.2
95h	3.1	B5h	6.3
96h	3.2	B6h	6.4
97h	3.3	B7h	6.5
98h	3.4	B8h	6.6
99h	3.5	B9h	6.7
9Ah	3.6	BAh	6.8
9Bh	3.7	BBh	6.9
9Ch	3.8	BCh	7
9Dh	3.9	BDh	7.1
9Eh	4	BEh	7.2
9Fh	4.1	BFh	7.3
A0h	4.2	C0h	7.4
A1h	4.3	C1h	7.5
A2h	4.4	C2h	7.6
A3h	4.5	C3h	7.7
A4h	4.6	C4h	7.8
A5h	4.7	C5h	7.9
A6h	4.8	C6h	8
A7h	4.9	C7h	8.1
A8h	5	C8h	8.2
A9h	5.1	C9h	8.3
AAh	5.2	CAh	8.4
ABh	5.3	CBh	8.5
ACh	5.4	CCh	8.6
ADh	5.5	Other	NA

A[7]/B[7] = 0,
VSH1/VSH2 voltage setting from 8.8V to 17V

A/B[7:0]	VSH1/VSH2	A/B[7:0]	VSH1/VSH2
21h	8.8	37h	13
23h	9	38h	13.2
24h	9.2	39h	13.4
25h	9.4	3Ah	13.6
26h	9.6	3Bh	13.8
27h	9.8	3Ch	14
28h	10	3Dh	14.2
29h	10.2	3Eh	14.4
2Ah	10.4	3Fh	14.6
2Bh	10.6	40h	14.8
2Ch	10.8	41h	15
2Dh	11	42h	15.2
2Eh	11.2	43h	15.4
2Fh	11.4	44h	15.6
30h	11.6	45h	15.8
31h	11.8	46h	16
32h	12	47h	16.2
33h	12.2	48h	16.4
34h	12.4	49h	16.6
35h	12.6	4Ah	16.8
36h	12.8	4Bh	17
		Other	NA

C[7] = 0,
VSL setting from -5V to -17V

C[7:0]	VSL
0Ah	-5
0Ch	-5.5
0Eh	-6
10h	-6.5
12h	-7
14h	-7.5
16h	-8
18h	-8.5
1Ah	-9
1Ch	-9.5
1Eh	-10
20h	-10.5
22h	-11
24h	-11.5
26h	-12
28h	-12.5
2Ah	-13
2Ch	-13.5
2Eh	-14
30h	-14.5
32h	-15
34h	-15.5
36h	-16
38h	-16.5
3Ah	-17
Other	NA

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	08	0	0	0	0	1	0	0	0	Initial Code Setting OTP Program	Program Initial Code Setting The command required CLKEN=1. Refer to Register 0x22 for detail. BUSY pad will output high during operation.

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	09	0	0	0	0	1	0	0	1	Write Register for Initial Code Setting	Write Register for Initial Code Setting Selection A[7:0] ~ D[7:0]: Reserved Details refer to Application Notes of Initial Code Setting
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
0	1		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	0A	0	0	0	0	1	0	1	0	Read Register for Initial Code Setting	Read Register for Initial Code Setting
0	0	0C	0	0	0	0	1	1	0	0	Booster Soft start Control	Booster Enable with Phase 1, Phase 2 and Phase 3 for soft start current and duration setting. A[7:0] -> Soft start setting for Phase1 = 8Bh [POR] B[7:0] -> Soft start setting for Phase2 = 9Ch [POR] C[7:0] -> Soft start setting for Phase3 = 96h [POR] D[7:0] -> Duration setting = 0Fh [POR] Bit Description of each byte: A[6:0] / B[6:0] / C[6:0]:
0	1		1	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		1	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		1	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
0	1		0	0	D_5	D_4	D_3	D_2	D_1	D_0		

Bit[6:4]	Driving Strength Selection
000	1(Weakest)
001	2
010	3
011	4
100	5
101	6
110	7
111	8(Strongest)

Bit[3:0]	Min Off Time Setting of GDR [Time unit]
0000 ~ 0011	NA
0100	2.6
0101	3.2
0110	3.9
0111	4.6
1000	5.4
1001	6.3
1010	7.3
1011	8.4
1100	9.8
1101	11.5
1110	13.8
1111	16.5

D[5:0]: duration setting of phase
D[5:4]: duration setting of phase 3
D[3:2]: duration setting of phase
D[1:0]: duration setting of phase 1

Bit[1:0]	Duration of Phase [Approximation]
00	10ms
01	20ms
10	30ms
11	40ms

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	10	0	0	0	1	0	0	0	0	Deep Sleep mode	Deep Sleep mode Control:
0	1		0	0	0	0	0	0	A_1	A_0		After this command initiated, the chip will enter Deep Sleep Mode, BUSY pad will keep output high. Remark: To Exit Deep Sleep mode, User required to send HWRESET to the driver
0	0	11	0	0	0	1	0	0	0	1	Data Entry mode setting	Define data entry sequence A[2:0] = 011 [POR]
0	1		0	0	0	0	0	A_2	A_1	A_0		A [1:0] = ID[1:0] Address automatic increment / decrement setting The setting of incrementing or decrementing of the address counter can be made independently in each upper and lower bit of the address. 00 –Y decrement, X decrement, 01 –Y decrement, X increment, 10 –Y increment, X decrement, 11 –Y increment, X increment [POR] A[2] = AM Set the direction in which the address counter is updated automatically after data are written to the RAM. AM= 0, the address counter is updated in the X direction. [POR] AM = 1, the address counter is updated in the Y direction.
0	0	12	0	0	0	1	0	0	1	0	SW RESET	It resets the commands and parameters to their S/W Reset default values except R10h-Deep Sleep Mode During operation, BUSY pad will output high. Note: RAM data are unaffected by this command.

Command Table

<table>
<tr><th>R/W#</th><th>D/C#</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>14</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td rowspan="2">HV Ready Detection</td><td>HV ready detection A[7:0] = 00h [POR]
The command required CLKEN=1 and ANALOGEN=1.
Refer to Register 0x22 for detail.
After this command initiated, HV Ready detection starts.
BUSY pad will output high during detection.
The detection result can be read from the Status Bit Read (Command 0x2F).</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>A_6</td><td>A_5</td><td>A_4</td><td>0</td><td>A_2</td><td>A_1</td><td>A_0</td><td>A[6:4]=n for cool down duration: 10ms x (n+1)
A[2:0]=m for number of Cool Down Loop to detect.
The max HV ready duration is 10ms x (n+1) x (m)
HV ready detection will be trigger after each cool down time. The detection will be completed when HV is ready.
For 1 shot HV ready detection, A[7:0] can be set as 00h.</td></tr>
<tr><td colspan="13"></td></tr>
<tr><td>0</td><td>0</td><td>15</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td rowspan="2">VCI Detection</td><td>VCI Detection</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>A_2</td><td>A_1</td><td>A_0</td><td>A[2:0] = 100 [POR] , Detect level at 2.3V
A[2:0] : VCI level Detect<table><tr><td>A[2:0]</td><td>VCI level</td></tr><tr><td>011</td><td>2.2V</td></tr><tr><td>100</td><td>2.3V</td></tr><tr><td>101</td><td>2.4V</td></tr><tr><td>110</td><td>2.5V</td></tr><tr><td>111</td><td>2.6V</td></tr><tr><td>Other</td><td>NA</td></tr></table>The command required CLKEN=1 and ANALOGEN=1
Refer to Register 0x22 for detail.
After this command initiated, VCI detection starts.
BUSY pad will output high during detection.
The detection result can be read from the Status Bit Read (Command 0x2F).</td></tr>
<tr><td colspan="13"></td></tr>
<tr><td>0</td><td>0</td><td>18</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td rowspan="2">Temperature Sensor Control</td><td rowspan="2">Temperature Sensor Selection
A[7:0] = 48h [POR], external temperature sensor
A[7:0] = 80h Internal temperature sensor</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td></tr>
<tr><td colspan="13"></td></tr>
<tr><td>0</td><td>0</td><td>1A</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td rowspan="2">Temperature Sensor Control (Write to temperature register)</td><td rowspan="2">Write to temperature register.
A[7:0] = 7Fh [POR]</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td></tr>
<tr><td colspan="13"></td></tr>
<tr><td>0</td><td>0</td><td>1B</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td rowspan="2">Temperature Sensor Control (Read from temperature register)</td><td rowspan="2">Read from temperature register.</td></tr>
<tr><td>1</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td></tr>
</table>

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	1C	0	0	0	1	1	1	0	0	Temperature Sensor Control (Write Command to External temperature sensor)	Write Command to External temperature sensor. A[7:0] = 00h [POR], B[7:0] = 00h [POR], C[7:0] = 00h [POR], A[7:6] A[7:6] – Select no of byte to be sent 00 – Address + pointer 01 – Address + pointer + 1st parameter 10 – Address + pointer + 1st parameter + 2nd pointer 11 – Address A[5:0] – Pointer Setting B[7:0] – 1st parameter C[7:0] – 2nd parameter The command required CLKEN=1. Refer to Register 0x22 for detail. After this command initiated, Write Command to external temperature sensor starts. BUSY pad will output high during operation.
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
0	0	20	0	0	1	0	0	0	0	0	Master Activation	Activate Display Update Sequence The Display Update Sequence Option is located at R22h. BUSY pad will output high during operation. User should not interrupt this operation to avoid corruption of panel images.
0	0	21	0	0	1	0	0	0	0	1	Display Update Control 1	RAM content option for Display Update A[7:0] = 00h [POR] B[7:0] = 00h [POR] A[7:4] Red RAM option 0000 – Normal 0100 – Bypass RAM content as 0 1000 – Inverse RAM content A[3:0] BW RAM option 0000 – Normal 0100 – Bypass RAM content as 0 1000 – Inverse RAM content B[7:6] Resolution select 00 – Display resolution is 200x384 01 – Display resolution is 184x384 10 – Display resolution is 168x384 11 – Display resolution is 216x384
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		B_7	B_6	0	0	0	0	0	0		

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	22	0	0	1	0	0	0	1	0	Display Update Control 2	Display Update Sequence Option: Enable the stage for Master Activation A[7:0]= FFh (POR)
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		(see Operating sequence table below)
0	0	24	0	0	1	0	0	1	0	0	Write RAM (Black White) / RAM 0x24	After this command, data entries will be written into the BW RAM until another command is written. Address pointers will advance accordingly For Write pixel: Content of Write RAM(BW) = 1 For Black pixel: Content of Write RAM(BW) = 0

Operating sequence	Parameter (in Hex)
Enable clock signal	80
Disable clock signal	01
Enable clock signal ➔ Enable Analog	C0
Disable Analog ➔ Disable clock signal	03
Enable clock signal ➔ Load LUT with DISPLAY Mode 1 ➔ Disable clock signal	91
Enable clock signal ➔ Load LUT with DISPLAY Mode 2 ➔ Disable clock signal	99
Enable clock signal ➔ Load temperature value ➔ Load LUT with DISPLAY Mode 1 ➔ Disable clock signal	B1
Enable clock signal ➔ Load temperature value ➔ Load LUT with DISPLAY Mode 2 ➔ Disable clock signal	B9
Enable clock signal ➔ Enable Analog ➔ Display with DISPLAY Mode 1 ➔ Disable Analog ➔ Disable OSC	C7
Enable clock signal ➔ Enable Analog ➔ Display with DISPLAY Mode 2 ➔ Disable Analog ➔Disable OSC	CF
Enable clock signal ➔Enable Analog ➔ Load temperature value ➔ DISPLAY with DISPLAY Mode 1 ➔ Disable Analog ➔ Disable OSC	F7
Enable clock signal ➔Enable Analog ➔ Load temperature value ➔ DISPLAY with DISPLAY Mode 2 ➔ Disable Analog ➔ Disable OSC	FF

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	26	0	0	1	0	0	1	1	0	Write RAM (RED) / RAM 0x26	After this command, data entries will be written into the RED RAM until another command is written. Address pointers will advance accordingly. For Red pixel: Content of Write RAM(RED) = 1 For non-Red pixel [Black or White]: Content of Write RAM(RED) = 0
0	0	27	0	0	1	0	0	1	1	1	Read RAM	After this command, data read on the MCU bus will fetch data from RAM. According to parameter of Register 41h to select reading RAM0x24/ RAM0x26, until another command is written. Address pointers will advance accordingly. The 1st byte of data read is dummy data.
0	0	2E	0	0	1	0	1	1	1	0	User ID Read	Read 30 Byte User ID stored in OTP: A[7:0]]~AD[7:0]: UserID (R38, Byte A and Byte AD) [30 bytes]
1	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
1	1		. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .		
1	1		Z_7	Z_6	Z_5	Z_4	Z_3	Z_2	Z_1	Z_0		
1	1		AA_7	AA_6	AA_5	AA_4	AA_3	AA_2	AA_1	AA_0		
1	1		AB_7	AB_6	AB_5	AB_4	AB_3	AB_2	AB_1	AB_0		
1	1		AC_7	AC_6	AC	AC_4	AC_3	AC_2	AC_1	AC_0		
1	1		AD_7	AD_6	AD_5	AD_4	AD_3	AD_2	AD_1	AD_0		
0	0	38	0	0	1	1	1	0	0	0	Write Register for User ID	Write Register for User ID A[7:0]]~AD[7:0]: UserID [30 bytes] Remarks: A[7:0]~AD[7:0] can be stored in OTP
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
0	1		. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .		
0	1		Z_7	Z_6	Z_5	Z_4	Z_3	Z_2	Z_1	Z_0		
0	1		AA_7	AA_6	AA_5	AA_4	AA_3	AA_2	AA_1	AA_0		
0	1		AB_7	AB_6	AB_5	AB_4	AB_3	AB_2	AB_1	AB_0		
0	1		AC_7	AC_6	AC	AC_4	AC_3	AC_2	AC_1	AC_0		
0	1		AD_7	AD_6	AD_5	AD_4	AD_3	AD_2	AD_1	AD_0		

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	3C	0	0	1	1	1	1	0	0	Border Waveform Control	Select border waveform for VBD A[7:0] = C0h [POR], set VBD as HIZ. A [7:6] :Select VBD option A[7:6] — Select VBD as 00 — GS Transition, Defined in A[2] and A[1:0] 01 — Fix Level, Defined in A[5:4] 10 — VCOM 11[POR] — HiZ A [5:4] Fix Level Setting for VBD A[5:4] — VBD level 00 — VSS 01 — VSH1 10 — VSL 11 — VSH2 A [1:0] GS Transition setting for VBD VBD Level Selection: 00b: VCOM ; 01b: VSH1; 10b: VSL; 11b: VSH2 A[1:0] — VBD Transition 00 — LUT0 01 — LUT1 10 — LUT2 11 — LUT3
0	1		A_7	A_6	A_5	A_4	0	0	A_1	A_0		
0	0	41	0	1	0	0	0	0	0	1	Read RAM Option	Read RAM Option A[0]= 0 [POR] 0 : Read RAM corresponding to RAM0x24 1 : Read RAM corresponding to RAM0x26
0	1		0	0	0	0	0	0	0	A_0		
0	0	44	0	1	0	0	0	1	0	0	Set RAM X - address Start / End position	Specify the start/end positions of the window address in the X direction by an address unit for RAM A[5:0]: XSA[5:0], XStart, POR = 00h B[5:0]: XEA[5:0], XEnd, POR = 18h
0	1		0	0	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		0	0	B_5	B_4	B_3	B_2	B_1	B_0		
0	0	45	0	1	0	0	0	1	0	1	Set Ram Y- address Start / End position	Specify the start/end positions of the window address in the Y direction by an address unit for RAM A[8:0]: YSA[8:0], YStart, POR = 000h B[8:0]: YEA[8:0], YEnd, POR = 17Fh
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		0	0	0	0	0	0	0	A_8		
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		0	0	0	0	0	0	0	B_8		

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	4E	0	1	0	0	1	1	1	0	Set RAM X address counter	Make initial settings for the RAM X address in the address counter (AC) A[5:0]: 00h [POR].
0	1		0	0	A_5	A_4	A_3	A_2	A_1	A_0		
0	0	4F	0	1	0	0	1	1	1	1	Set RAM Y address counter	Make initial settings for the RAM Y address in the address counter (AC) A[8:0]: 000h [POR].
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		0	0	0	0	0	0	0	A_8		
0	0	7F	0	1	1	1	1	1	1	1	NOP	This command is an empty command; it does not have any effect on the display module. However, it can be used to terminate Frame Memory Write or Read Commands.

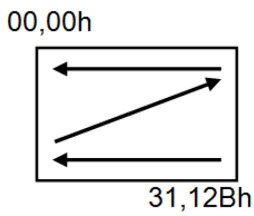
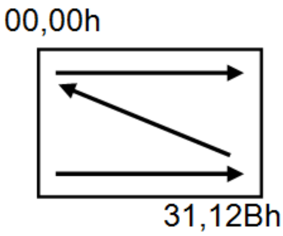
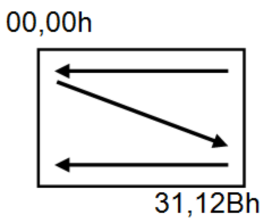
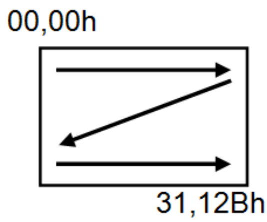
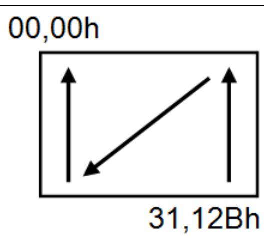
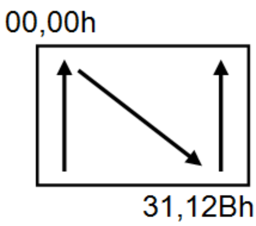
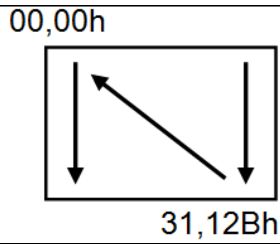
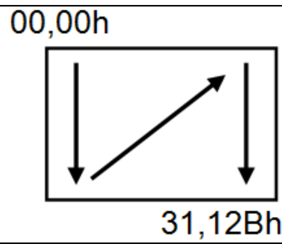
10.Data Entry Mode Setting (11h)

This command has multiple configurations and each bit setting is described as follows:

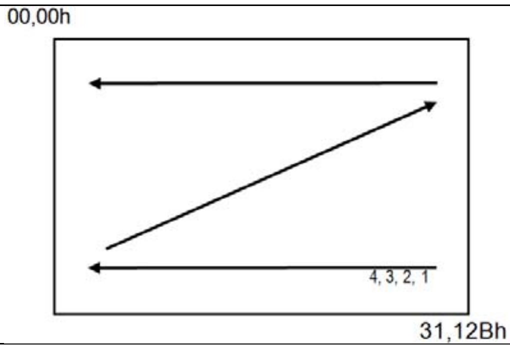
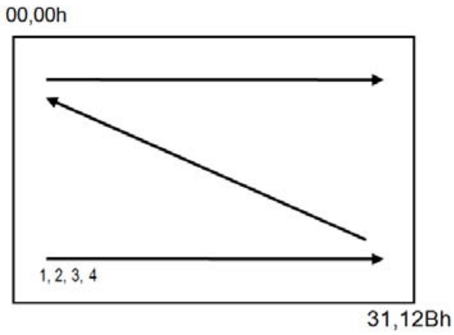
R/W	DC	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1						AM	ID1	IDO
POR		0	0	0	0	0	0	1	1

ID[1:0]: The address counter is automatically incremented by 1, after data is written to the RAM when ID[1:0] = “01”. The address counter is automatically decremented by 1, after data is written to the RAM when ID[1:0] = “00”. The setting of incrementing or decrementing of the address counter can be made independently in each upper and lower bit of the address. The direction of the address when data is written to the RAM is set by AM bits.

AM: Set the direction in which the address counter is updated automatically after data are written to the RAM. When AM = “0”, the address counter is updated in the X direction. When AM = “1”, the address counter is updated in the Y direction. When window addresses are selected, data are written to the RAM area specified by the window addresses in the manner specified with ID[1:0] and AM bits.

	ID [1:0]="00" X: decrement Y: decrement	ID [1:0]="01" X: increment Y: decrement	ID [1:0]="10" X: decrement Y: increment	ID [1:0]="11" X: increment Y: increment
AM="0" X-mode				
AM="1" Y-mode				

The pixel sequence is defined by the ID [0],

	ID [1:0]="00" X: decrement Y: decrement	D [1:0]="01" X: increment Y: decrement
AM="0" X-mode		

11. Reference Circuit

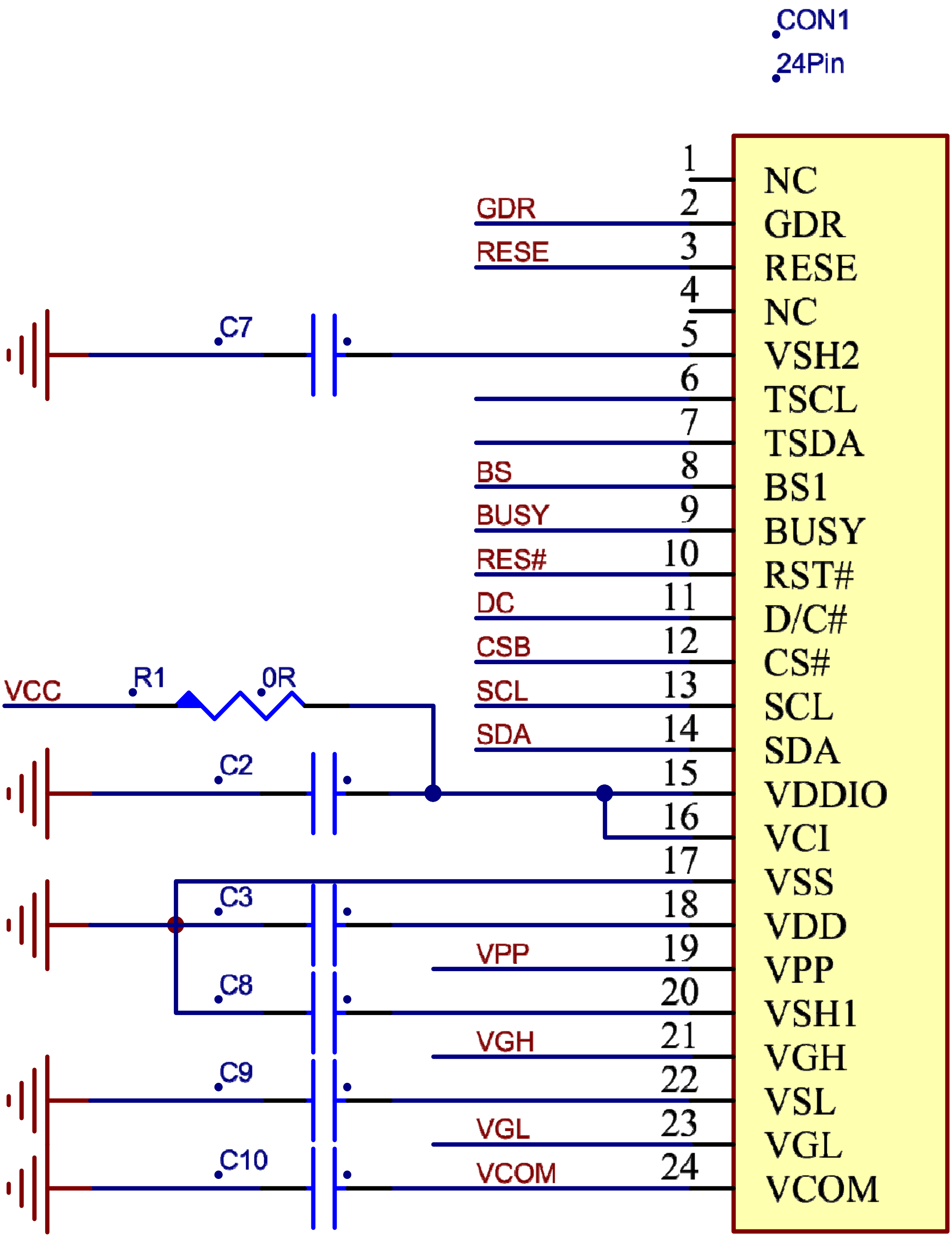


Figure. 11-1

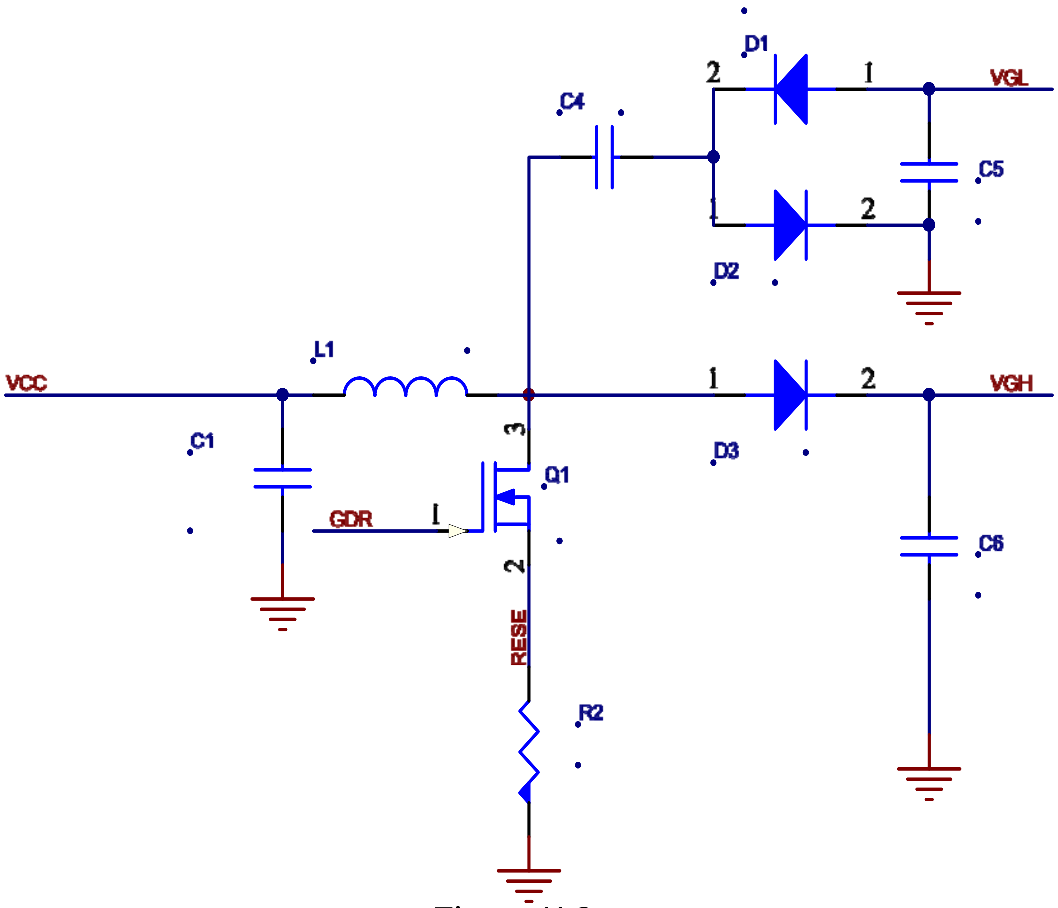


Figure. 11-2

Part Name	Value /requirement/Reference Part
C1—C9	1uF/0603;X5R;Voltage Rating: 25V
C10	1uF/0603;X7R;Voltage Rating: 25V
D1—D3	MBR0530 1) Reverse DC voltage≥30V 2) Forward current≥500mA 3)Forward voltage≤430mV
R2	2.2 Ω/0603： 1% variation
Q1	NMOS:Si1304BDL/NX3008NBK 1） Drain-Source breakdown voltage ≥30V 2） Vgs（th）=0.9（Typ）, 1.3V（Max） 3） Rds on≤ 2.1 Ω @ Vgs=2.5V
L1	47uH/NRH3010T470MN Maximum DC current~420mA Maximum DC resistance~650mΩ
CON24Pin	0.5mm ZIF Socket 24Pins,0.5mm pitch

12. ABSOLUTE MAXIMUM RATING

Table 12-1: Maximum Ratings

Symbol	Parameter	Rating	Unit	Humidity	Unit	Note
V_{CI}	Logic supply voltage	-0.5 to +6.0	V	-	-	
T_{OPR}	Operation temperature range	0 to 50	°C	35 to70	%	
Tttg	Transportation temperature range	-25 to 60	°C	-	-	Note12-2
Tstg	Storage condition	0 to 40	°C	35 to70	%	Maximum storage time: 5 years

Note 12-1:Maximum ratings are those values beyond which damages to the device may occur.
Functional operation should be restricted to the limits in the Electrical Characteristics chapter.
Note12-2: Tttg is the transportation condition, the transport time is within 10 days for -25℃~0℃ or 50℃~60℃.

13.DC CHARACTERISTICS

The following specifications apply for: VSS=0V, VCI=3.0 V, T_{OPR}=25℃.

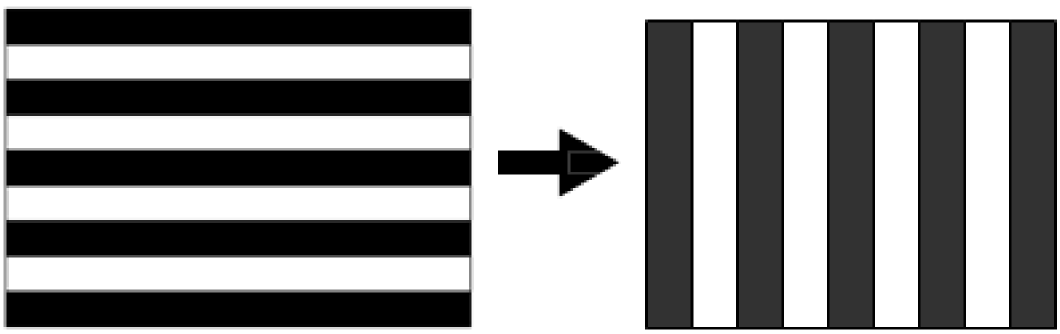
Table 13-1: DC Characteristics

Symbol	Parameter	Test Condition	Applicable pin	Min.	Typ.	Max.	Unit
VCI	VCI operation voltage		VCI	2.5	3	3.7	V
VIH	High level input voltage		SDA, SCL, CS#, D/C#, RES#, BS1	0.8VDDIO			V
VIL	Low level input voltage					0.2VDDIO	V
VOH	High level output voltage	IOH = -100uA	BUSY	0.9VDDIO			V
VOL	Low level output voltage	IOL = 100uA				0.1VDDIO	V
Iupdate	Module operating current			-	3	-	mA
Isleep	Deep sleep mode	VCI=3 V		-	-	3	uA

The Typical power consumption is measured using associated 25℃ waveform with following pattern transition: from horizontal scan pattern to vertical scan pattern. (Note 13-1)
- The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by XingTai.
- Vcom value will be OTP before in factory or present on the label sticker.

Note 13-1

The Typical power consumption



14. Serial Peripheral Interface Timing

The following specifications apply for: VSS=0V, VCI=2.5V to 3.7V, T_{OPR}=25℃ , CL=20pF

Write mode

Symbol	Parameter	Min	Typ	Max	Unit
fSCL	SCL frequency (Write Mode)	-	-	20	MHz
tCSSU	Time CS# has to be low before the first rising edge of SCLK	60	-	-	ns
tCSHLD	Time CS# has to remain low after the last falling edge of SCLK	65	-	-	ns
tCSHIGH	Time CS# has to remain high between two transfers	100	-	-	ns
tSCLHIGH	Part of the clock period where SCL has to remain high	25	-	-	ns
tSCLLOW	Part of the clock period where SCL has to remain low	25	-	-	ns
tSISU	Time SI (SDA Write Mode) has to be stable before the next rising edge of SCL	10	-	-	ns
tSIHLD	Time SI (SDA Write Mode) has to remain stable after the rising edge of SCL	40	-	-	ns

Read mode

Symbol	Parameter	Min	Typ	Max	Unit
fSCL	SCL frequency (Read Mode)	-	-	2.5	MHz
tCSSU	Time CS# has to be low before the first rising edge of SCLK	100	-	-	ns
tCSHLD	Time CS# has to remain low after the last falling edge of SCLK	50	-	-	ns
tCSHIGH	Time CS# has to remain high between two transfers	250	-	-	ns
tSCLHIGH	Part of the clock period where SCL has to remain high	180	-	-	ns
tSCLLOW	Part of the clock period where SCL has to remain low	180	-	-	ns
tSOSU	Time SO(SDA Read Mode) will be stable before the next rising edge of SCL	-	50	-	ns
tSOHLD	Time SO (SDA Read Mode) will remain stable after the falling edge of SCL	-	0	-	ns

Note: All timings are based on 20% to 80% of VDDIO-VSS

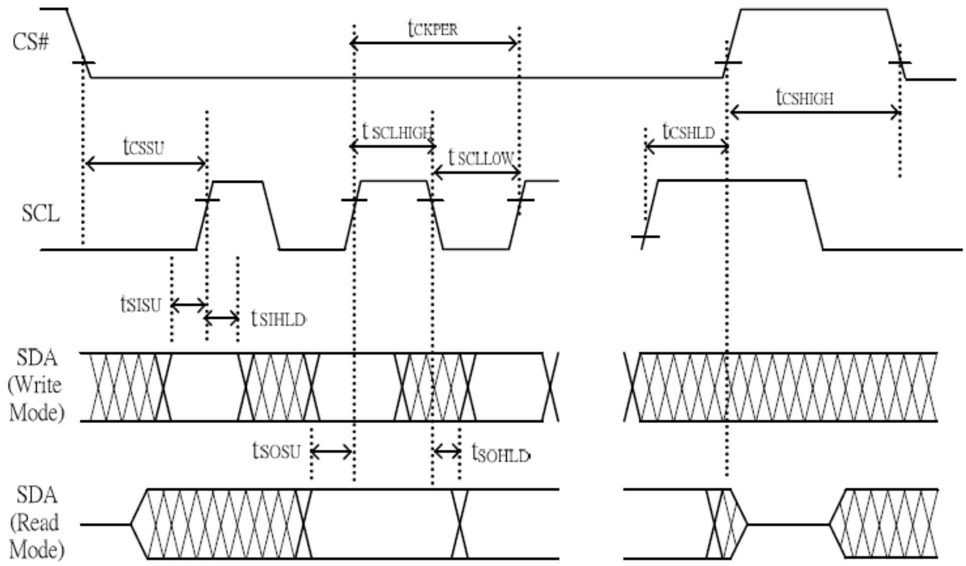


Figure 14-1: SPI timing diagram

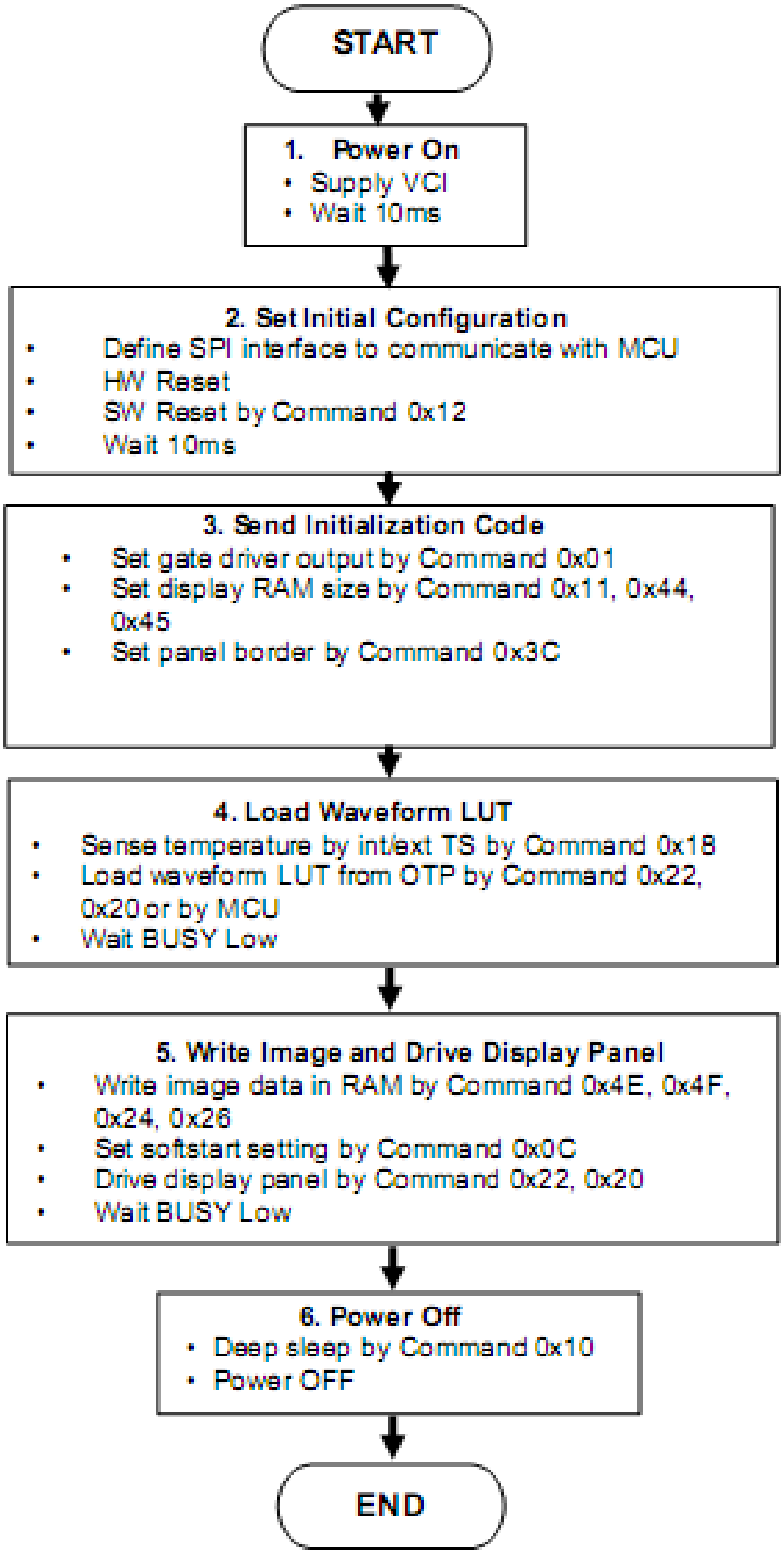
15. Power Consumption

Parameter	Symbol	Conditions	TYP	Max	Unit	Remark
Panel power consumption during update	-	25℃	-	30	mAs	-
Deep sleep mode	-	25℃	-	3	uA	-

MAS=update average current ×update time

16.Typical Operating Sequence

16.1 Normal Operation Flow



17.Optical characteristics

17.1 Specifications

Measurements are made with that the illumination is under an angle of 45 degrees, the detection is perpendicular unless otherwise specified.

T=25±3℃，VCI=3.0V

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT	Note
R	Reflectance	White	30	35	-	%	Note 17-1
Gn	2Grey Level	-	-	KS+(WS-KS)×n(m-1)	-	L*	-
CR	Contrast Ratio	-	-	10	-	-	-
KS	Black State L* value	-	-	18	-	-	Note 17-1
	Black State a* value	-	-	0.2	-	-	Note 17-1
WS	White State L* value	-	-	67	-	-	Note 17-1
Panel	Image Update	Storage and transportation	-	Update the white screen	-	-	-
	Update Time	Operation	-	Suggest Updated once a day	-	-	-

WS : White state, KS : Black State,

Note 17-1 : Luminance meter : i - One Pro Spectrophotometer

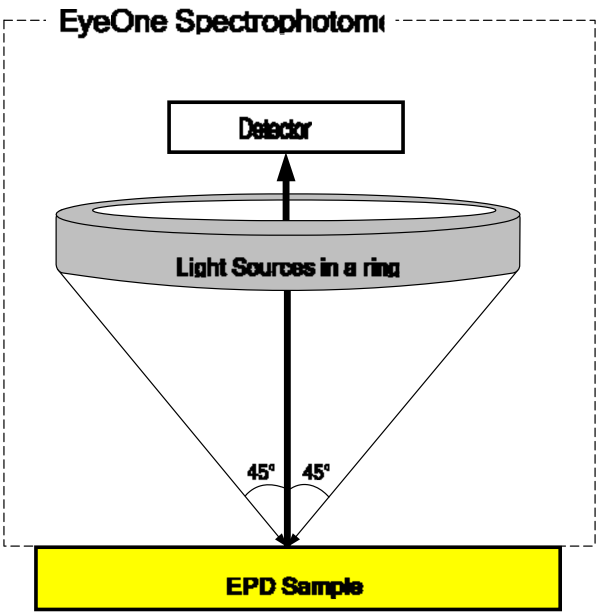
Note 17-2: We guarantee display quality from 0℃～30℃ generally, If operation ambient temperature from 0℃～50℃, will offer special waveform by Xingtai.

17.2 Definition of contrast ratio

The contrast ratio (CR) is the ratio between the reflectance in a full white area (R1) and the reflectance in a dark area (Rd)() :

R1: white reflectance Rd: dark reflectance

CR = R1/Rd

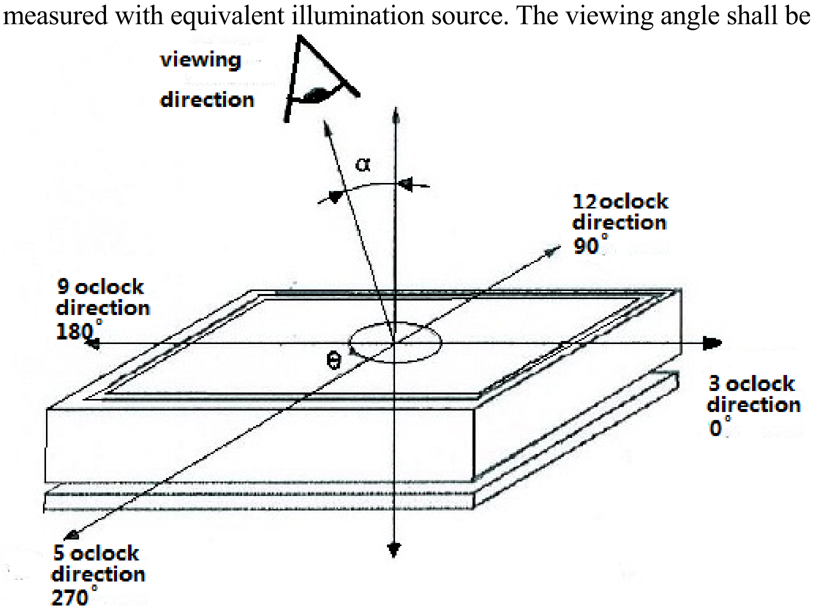


17.3 Reflection Ratio

The reflection ratio is expressed as:

R = Reflectance Factor $_{\text{white board}}$ x (L $_{\text{center}}$ / L $_{\text{white board}}$)

L $_{\text{center}}$ is the luminance measured at center in a white area (R=G =B=1). L $_{\text{white board}}$ is the luminance of a standard white board. Both are measured with equivalent illumination source. The viewing angle shall be no more than 2 degrees.



18. HANDLING, SAFETY AND ENVIROMENTAL REQUIREMENTS

WARNING
The display module should be kept flat or fixed to a rigid, curved support with limited bending along the long axis. It should not be used for continual flexing and bending. Handle with care. Should the display break do not touch any material that leaks out. In case of contact with the leaked material then wash with water and soap.

CAUTION
The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.
Disassembling the display module can cause permanent damage and invalidate the warranty agreements.
IPA solvent can only be applied on active area and the back of a glass. For the rest part, it is not allowed.
Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged . Moreover the display is sensitive to static electricity and other rough environmental conditions.

Mounting Precautions
(1) It`s recommended that you consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the module.
(2) It`s recommended that you attach a transparent protective plate to the surface in order to protect the EPD. Transparent protective plate should have sufficient strength in order to resist external force.
(3) You should adopt radiation structure to satisfy the temperature specification.
(4) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the PS at high temperature and the latter causes circuit break by electro-chemical reaction.
(5) Do not touch, push or rub the exposed PS with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment. Do not touch the surface of PS for bare hand or greasy cloth. (Some cosmetics deteriorate the PS)
(6) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach the PS. Do not use acetone, toluene and alcohol because they cause chemical damage to the PS.
(7) Wipe off saliva or water drops as soon as possible. Their long time contact with PS causes deformations and color fading.

Data sheet status	
Product specification	The data sheet contains final product specifications.

Limiting values
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.
Application information
Where application information is given, it is advisory and dose not form part of the specification.

Product Environmental certification
ROHS
REMARK
All The specifications listed in this document are guaranteed for module only. Post-assembled operation or component(s) may impact module performance or cause unexpected effect or damage and therefore listed specifications is not warranted after any Post-assembled operation.

19. Reliability test

19.1 Reliability test items

	TEST	CONDITION	REMARK
1	High-Temperature Operation	T=40℃，RH=35%RH，For 240Hr	
2	Low-Temperature Operation	T = 0℃ for 240 hrs	
3	High-Temperature Storage	T=60℃ RH=35%RH For 240Hr	Test in white pattern
4	Low-Temperature Storage	T = -25℃ for 240 hrs	Test in white pattern
5	High Temperature, High-Humidity Operation	T=40℃，RH=90%RH，For 168Hr	
6	High Temperature, High-Humidity Storage	T=60℃，RH=80%RH，For 240Hr	Test in white pattern
7	Temperature Cycle	-25℃(30min)~70℃(30min)，100 Cycle	Test in white pattern
8	Package Vibration	1.04G,Frequency : 20~200Hz Direction : X,Y,Z Duration: 30 minutes in each direction	Full packed for shipment
9	Package Drop Impact	Drop from height of 100 cm on Concrete surface Drop sequence:1 corner, 3edges, 6face One drop for each.	Full packed for shipment
10	UV exposure Resistance	765 W/㎡ for 168hrs,40℃	
11	Electrostatic discharge	Machine model: +/-250V,0Ω,200pF	

Actual EMC level to be measured on customer application.

Note1：Stay white pattern for storage and non-operation test.

Note2：Operation is black/white pattern , hold time is 150S.

Note3：The function, appearance should meet the requirements of the test before and after the test.

Note4：Keep testing after 2 hours placing at 20℃-25℃.

19.2 Product life time

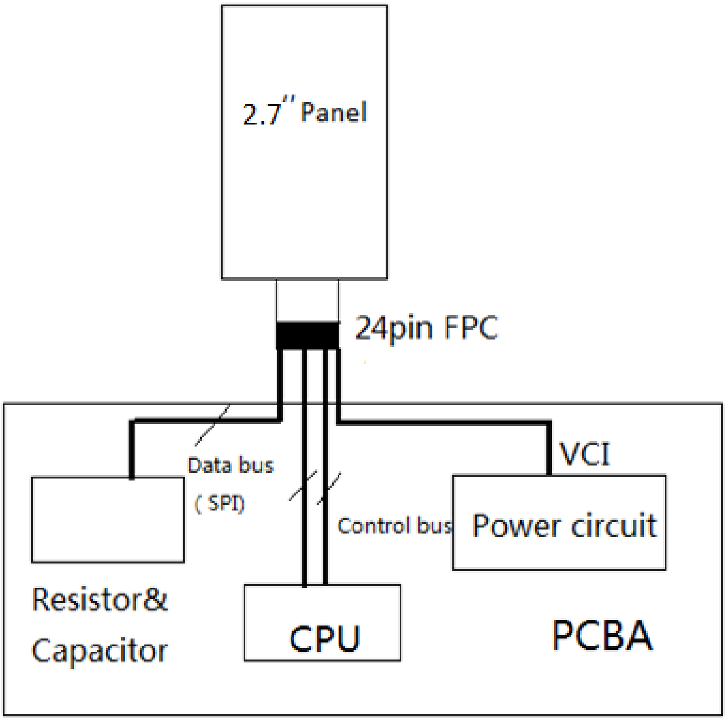
The EPD Module is designed for a 5-year life-time with 25 ℃/50%RH operation assumption. Reliability estimation testing with accelerated life-time theory would be demonstrated to provide confidence of EPD lifetime.

19.3 Product warranty

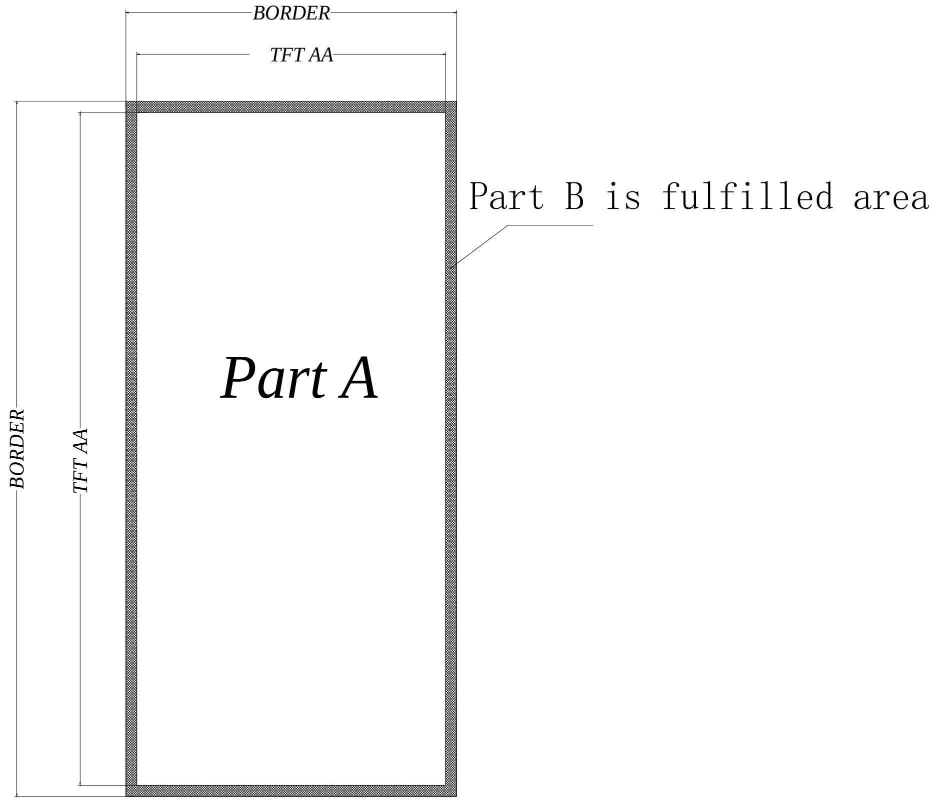
Warranty conditions have to be negotiated between Xingtai and individual customers.

Xingtai provides 12+1(one month delivery time) months warranty for all products which are purchased from Xingtai.

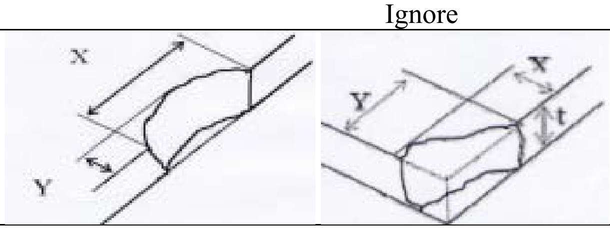
20. Block Diagram

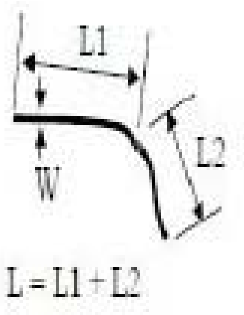


21. PartA/PartB specification



22. Point and line standard

Shipment Inspection Standard						
Equipment：Electrical test fixture, Point gauge						
Outline dimension	43.79(H)×69.72(V)×0.9(D)	Unit：㎜	Part-A	Active area	Part-B	Border area
Environment	Temperature	Humidity	Illuminance	Distance	Time	Angle
	19℃～25℃	55%±5%RH	800～1300Lux	300 ㎜	35Sec	
Defect type	Inspection method	Standard		Part-A		Part-B
Spot	Electric Display	D≤0.25 ㎜		Ignore		Ignore
		0.25 ㎜<D≤0.4 ㎜		N≤4		Ignore
		D>0.4 ㎜		Not Allow		Ignore
Display unwork	Electric Display	Not Allow		Not Allow		Ignore
Display error	Electric Display	Not Allow		Not Allow		Ignore
Scratch or line defect(include dirt)	Visual/Film card	L≤2 ㎜,W≤0.2 ㎜		Ignore		Ignore
		2.0mm<L≤5.0mm,0.2<W≤0.3mm,		N≤2		Ignore
		L>5 ㎜,W>0.3 ㎜		Not Allow		Ignore
PS Bubble	Visual/Film card	D≤0.2mm		Ignore		Ignore
		0.2mm≤D≤0.35mm		N≤4		Ignore
		D>0.35 mm		Not Allow		Ignore
Side Fragment	Visual/Film card	X≤6mm,Y≤0.4mm, Do not affect the electrode circuit (Edge chipping) X≤1mm,Y≤1mm, Do not affect the electrode circuit((Corner chipping) Ignore				
						
Remark	1. Appearance defect should not cause electrical defects；					
	2. Appearance defects should not cause dimensional accuracy problems					
	L=long W=wide D=point size N=Defects NO					



Line Defect

Spot Defect

L=long W=wide D=point size

23.Barcode

23.1 label appearance

ABBBBBBBCC
DDDEEEFGGG

23.2 QR scanned information（Total 28 code number+ 2 blank spaces）

A BBBBBBB CC □ DDD EEE F GGG □ H III JJ KK
① ② ③ ④ ⑤ ⑥ ⑦ ⑧ ⑨ ⑩ ⑪

① A——The factory code
② BBBBBBB——Module name of EPD
③ CC——Production line
④ DDD——Date of production
⑤ EEE——Production lot
⑥ F——Separator
⑦ GGG——FPL Lot
⑧ H——Product status
⑨ III——TFT、PS、EC.
⑩ JJ——IC
⑪ KK——Serial NO.
□ blank spaces

24. Packing

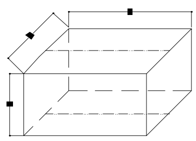
Packing Spec

Sheet No :

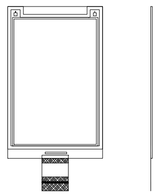
HOLITECH	Part No	HINK-E027A**	DATE	2018.06.26	VER	A0	Page	2-1

一，Package Type: Box

Box No	HINK-E029A01-ZX-A0
Box size	515*322*170
Containment	252PCS



PRODUCT DRAWING

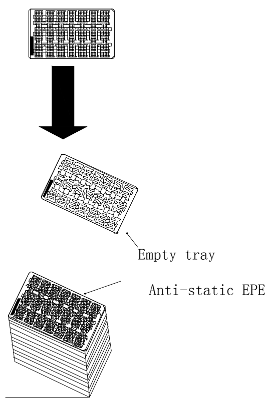


二,Inside package type:Plastic Tray

unit: mm

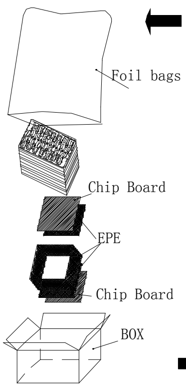
Plastic Tray	465*280*15	13 pcs
Anti-static foil bags	700*530*0.1	1 pcs
EPE(inside)	405.5*250.4*2	12 pcs
EPE(Up-Down)	485*145*10	2 pcs
EPE(Left-Right)	285*480*10	2 pcs
EPE(Front-back)	310*145*10	2 pcs
Chip board	500*306*5	2 pcs
Quantity/tray	21 pcs	
Tray number/sheet	12+1 Sheets	
Box	1	

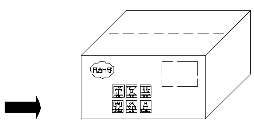
Step 1:
Material: Tray, EPE
Put the product in to the tray and keep the dispaly side up. Then put anti-static EPE in to each holes.



Step 2:
1) Must keep the angle 180 degree placed between the neighboring Plastic trays.
2) There are 12 layers product,total14*12=168pcs。
3) An empty Plastic tray intersects put on the top of the plastic trays.

Step 3:
1) In each case,put 2 bags of desiccant.then seal the trays with adhesive tapes.
2) Put the trays into foil bags.
3) heat seal the foil bags.





Step 4:
1)First put a chip board on the buttom of the box,then placed the down EPE, the left - right and front -back EPE.
2) Placed the sealed products into the box.
3) The last placed the up EPE on the top of the trays,and place a chip board on it.

Step 5:
1) Seal the box with adhensive tapes 。
2) Paste the lable onto the exterior box, and the lable can't cover the safety ,
transfer and RoSH sign。

Design	Z.Z.Q	Approve	H.Z.P	Confirm	X.X.M
Date	2018.06.26	Date	2018.6.26	Date	2018.6.26